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Modeling and Analysis of a Discontinuous-Conduction Mode (DCM) Controlled Flyback Converter with Variable Output Voltage

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Monografia apresentada ao Departamento de Engenharia Elétrica do Centro de Ciências Exatas e Tecnológicas da Universidade Federal de Viçosa, para a obtenção dos créditos da disciplina ELT 402 – Projeto de Engenharia II – e cumprimento do requisito parcial para obtenção do grau de Bacharel em Engenharia Elétrica.

Orientador Prof. Heverton Augusto Pereira

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Este trabalho é dedicado à minha família,
mentores e amigos.

Agradecimentos

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"Como um homem poder ser corajoso se está com medo? - Essa é a única altura em que um homem pode ser corajoso." (George Martin)

Resumo

As fontes Flyback são uma das topologias de fontes chaveadas utilizadas quando é desejado converter níveis de tensão onde um nível primário (geralmente alta tensão) é convertido para o secundário (baixa tensão), através da associação do chaveamento de um transitor, em série com um acoplamento indutivo, e os efeitos da polarização do diodo. Esses conversores são destinados, majoritariamente, a retificadores CA/CC para aparelhos eletrônicos, carregadores de baterias e fontes de tensão auxiliares em aplicações de até 150 W. Nesse sentido, este trabalho reside no projeto, simulação e análise de um conversor Flyback com saída variável para o carregamento de associações de células de baterias de lítio com especificações de 3,6 V e 3,35 Ah em série, baseando-se na bateria NCR18650B da marca *Panasonic*. As características utilizadas para o dimensionamento dos componentes do circuito bem como as características de seu funcionamento são apresentadas, enfatizando a adaptação do circuito de controle de corrente e tensão para obter o padrão de curvas para carregamento de baterias e a variação do valor de tensão de saída. Dessa forma, através do software *PLECS*, é realizado a implementação e análise da proposta de um conversor de 34,125 W de potência máxima com valor da tensão de entrada de 100 V a 240 V eficazes, tensão contínua de saída entre 12,6 V e 21 V e valor de corrente média 1,625 A de saída, operando no Modo de Condução Descontínuo (DCM). O sistema foi submetido à diferentes padrões de carga para obtenção das curvas de corrente e tensão de saída com intuito de validar a proposta de controle.

Palavras-chaves: Flyback; Fontes Chaveadas; Baterias; Controle de Tensão; Controle de Corrente.

Abstract

Flyback power supplies are one of the most used Switch-Mode Power Supplies (SMPS), mostly when it is desired to convert voltage levels where a primary side level (often the the high voltage) is converted into a secondary (low voltage), which is obtained by the combined effects of a switching transistor in series with a coupled inductor, and the polarization characteristics of a diode. These converters are mostly seen in AC/DC adapters for electronic devices, battery chargers and auxiliary power supplies, typically less than 150 W. Hence, this work approaches the development, simulation and analysis of a variable output Flyback converter to charge combinations of series 3.6 V and 3.35 Ah battery cells, based on the NCR18650B, developed by *Panasonic*. It is presented the characteristics and references used for calculating the circuit components as well as its working nuances, stressing the feedback voltage-control and current control circuit adaptation in order to achieve the battery charging waves and output voltage variation. Thus, the software *PLECS* is used to implement and analyze the proposal of a 34.125 W prototype with the input voltage ranging from 100 V to 240 V, 12.6 V to 21 V output voltage and a maximum current of 1.625 A, while operating in the Discontinuous-Conduction Mode (DCM). Different load parameters were applied to the system in order to validate the general Flyback operation and the feedback control proposed.

Key-words: Flyback; SMPS; Batteries; Voltage-Control; Current-Control.

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List of abbreviations and acronyms

CC-CV	Constant-Current Constant-Voltage
CCM	Continuous-Conduction Mode
CTR	Current Transfer Ratio
DC	Direct Current
DCM	Discontinuous-Conduction Mode
EMI	Electromagnetic Interference
EV	Electric Vehicles
FET	Field-Effect Transistor
IC	Integrated Circuit
LED	Light Emitting Diode
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCMC	Peak Current Mode Control
PWM	Pulse-Width Modulation
RMS	Root-Mean-Square
SMPS	Switch-Mode Power Supplies

List of symbols

C_{clamp}	RCD Snubber Clamp Capacitor
C_{damp}	RC Snubber Damp Capacitor
C_{inmin}	Minimum Input Capacitance
C_o	Output Capacitance
C_{oss}	Drain-Source Capacitance
C_{prim}	Primary Winding Capacitance
CTR	Current Transfer Ratio
CTR_{min}	Minimum Current Transfer Ratio
D_{max}	Maximum Duty Cycle
ΔV_{in}	Input Voltage Ripple
ΔV_o	Output Voltage Ripple
D	Duty Cycle
f_c	Cross-over Frequency
f_r	Parasitic Resonant Frequency
f_{sw}	Switching Frequency
$G_c(s)$	Compensator Transfer Function
$G(s)$	Loop Gain Transfer Function
$G_{vd}(S)$	Converter Transfer Function
$H(s)$	Sensor Gain Transfer Function
I_C	Optocoupler's Collector Current
$I_{C_{max}}$	Maximum Optocoupler's Collector Current
I_F	Forward-biased LED Current
I_{fc}	Full Charging Current

I_o	Output Current
I_{o-avg}	Average Secondary Current
$I_{o_{max}}$	Maximum Output Current
I_{pk}	Peak Current Value Through the Primary Side Inductor
$I_{pk_{max}}$	Maximum Primary Side Peak Current
$I_{pk_{rms}}$	Maximum Primary Side Peak RMS Current
i_L	Inductor Current
$i_{load}(t)$	Load Current
L_p	Primary Side Inductance
L_{pmax}	Maximum Primary Side Inductance
N_p	Number of Turns on Primary Side Inductor
N_s	Number of Turns on Secondary Side Inductor
$P_{o_{max}}$	Maximum Output Power
R_1	Resistive-Divider Upper Resistor
R_{bias}	Biasing LED Resistor
R_{clamp}	RCD Snubber Clamp Resistor
R_{damp}	RC Snubber Damp Resistor
R_{ESR}	Capacitor's Equivalent Series Resistor
R_{LED}	LED Current-Limiting Resistor
$R_{LED_{max}}$	Maximum LED Current-Limiting Resistor
R_{lower}	Resistive-Divider Lower Resistor
R_{pullup}	Pull-up Resistor
$R_{RS_{max}}$	Maximum Current Sense Resistance
S_e	Slope of Compensation
S_f	Slope of MOSFET Current During Off Time
S_n	Slope of MOSFET Current During On Time

T_s	Switching Period
η	Efficiency
$V_{CE_{sat}}$	Optocoupler Transistor's Saturation Voltage
V_{cs}	Current Sense Voltage
$V_{ds_{max}}$	*Flat-top* Voltage Across the MOSFET
$V_{ds_{on}}$	Conducting MOSFET's Voltage
$V_{ds_{peak}}$	Drain-Source Spike Voltage
$V_{err}(s)$	Error Signal Voltage
V_F	Forward-biased LED Voltage
$V_{in_{max}}$	Maximum Input Voltage
$V_{in_{min}}$	Minimum Input Voltage
V_m	PWM Controller Gain
V_o	Output Voltage
$V_{o_{max}}$	Maximum Output Voltage
V_{out}	Controlled Output Voltage
$V_{piv_{max}}$	*Flat-top* Voltage Across the Diode
V_{ramp}	Slope Compensation Voltage
V_{ref}	Reference Voltage
V_{RS}	Current Sense Resistor's Voltage
V_{TL431}	TL431 Cathode Voltage
$V_{TL431_{min}}$	Minimum TL431 Cathode Voltage
v_c	Compensator Output
$v_e(s)$	Error Signal
$v_g(t)$	Input Line Voltage
v_s	Frequency Domain Output Voltage
v_t	Time Domain Output Voltage

x	Minimum Desired Idle Time
ϕ_m	Phase Margin

Contents

1 Introduction

Portable devices have become one of the main applications in the field of advanced technology, due to their small size, light weight and recharge capacity (CHEN; RINCÓN-MORA, 2006). Henceforth, battery-operated devices is now an integral element of modern life. In such applications, it is more practical and cost-effective to use rechargeable battery cells, avoiding to replace the batteries frequently. Thus, battery chargers have a key role in the power management system of such devices. The main key to create an effective charger involves the charging algorithm, i.e. the procedure by which the battery is charged, and its circuit implementation (TAR; FAYED, 2016).

Li-ion batteries are mostly used due to its advantages over different technologies, which includes high energy density, low maintenance, high voltage, absence of memory effect and the quantity of types available. Accordingly, Li-ion battery chargers are utensils that regulate battery charging current and voltage, commonly used for portable devices such as cellphones, laptops and tablets. Nevertheless, as mentioned previously, there must be a charging algorithm, or charging strategy, in order to avoid overcharging and preserve the rechargeable battery's life. In that sense, the most implemented charging technique for Li-ion batteries is the Constant-Current Constant-Voltage (CC-CV) charging profile that is automatically adjusted depending on the battery's temperature and voltage levels (OUREMCHI et al., 2018; SPORCK, 2022).

The CC-CV charging method consists mainly of three phases, as shown in Figure 1. The first stage, depicted as the trickle-charge phase, is designed to test if any defect has occurred to the battery cells, whether they are functioning properly, or they have been damaged. This is accomplished by applying a constant charging current, limited to around 1/10 of the full charging current (I_{fc}), to the battery for a predetermined period and measuring the battery cells voltage change. When it is determined if the battery is responding as expected to the applied current, the second charge stage starts. In the constant-current phase, the level of the charging current applied to the battery is increased to its full level, and the battery voltage is observed. This stage is maintained until the battery voltage reaches its maximum level, which normally corresponds to about 70% of the battery capacity. If the constant-current phase were to proceed up to 100% capacity it would cause the battery voltage to surpass its maximum rated level, which damages the battery and causes excessive heating. Hence, the constant-current phase must be stopped, and it is followed by the third phase. In the constant-voltage phase, the maximum battery voltage is controlled so the battery calls can reach its full capacity avoiding defects, during which time the battery current is observed. In this stage, the battery chemical structure determines how much current it can absorb to continue the charging process. Therefore,

as the battery continues to charge, its current starts to drop, and when the current reaches the trickle-charging level the constant-voltage phase is stopped and the battery is considered fully charged. It is important to mention that CC-CV chargers can incorporate additional phases as well. One of them is the top-off phase, it adds a constant-voltage phase, and is used only if the battery continues connected to a power source after it is fully charged. In this stage, the battery voltage is monitored, and once it drops slightly below its rated maximum level (caused by leakage or loading), a constant-voltage charging phase is activated for brief period to ensure the battery is fully charged while a power source is available. Consequently, the CC-CV charging method precisely controls the charging current and voltage levels, and it is a very popular and reliable charging scheme for batteries that are sensitive to voltage or current levels, such as Li-ion batteries (TAR; FAYED, 2016).

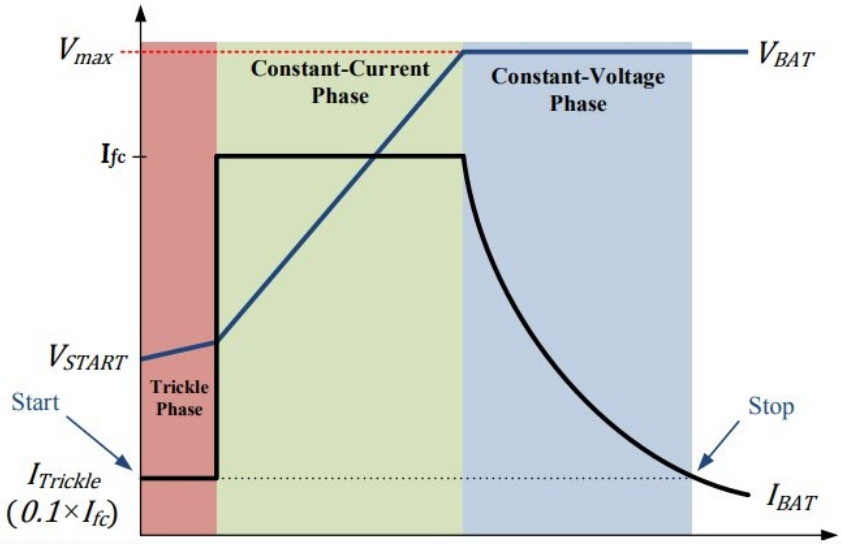

Figure 1 – The CC-CV charging profile. From: (TAR; FAYED, 2016).

The CC-CV charging configuration encompasses multiple phases that require the application and control of current and voltage levels. Thus, CC-CV chargers could be implemented using simple linear current and voltage sources, yet such a design would suffer from poor efficiency that is characteristic of linear implementations, which leads to high heat generation and reduces the amount of charge that can be delivered to the battery, resulting in a longer charging time. As an alternative, CC-CV chargers could be implemented using switching current and voltage sources, such as the buck converter represented in Figure 2. Using Switched-Mode Power Supplies (SMPS) bring the advantage of generating less heat and maximizing the charge that can be delivered to the battery from energy-limited sources. Nonetheless, these topologies tend to be bulky and more expensive due to passive components required for the converter, and may cause Electromagnetic Interference (EMI) issues due to switching (TAR; FAYED, 2016).

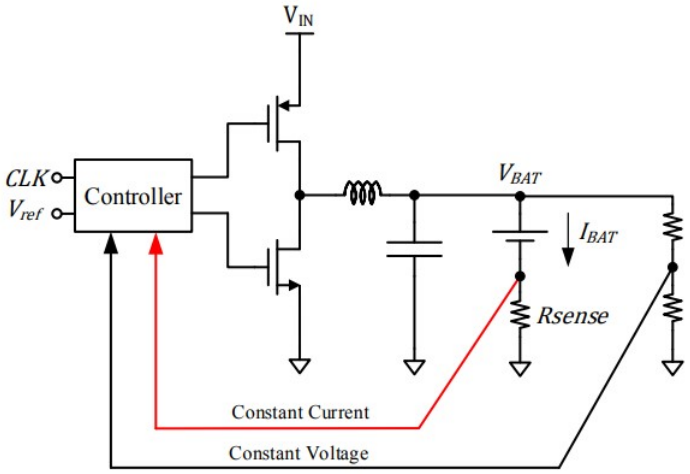

Figure 2 – Switching implementation of the CC-CV charging scheme using a single buck converter for the constant-current and constant-voltage phases. From: (TAR; FAYED, 2016).

The SMPS are basically DC-DC converters that can be divided into two types, the isolated DC-DC converter and the non-isolated DC-DC converter. The main characteristic of isolated DC-DC converters resides in the presence of an electrical barrier established by using a high frequency transformer in between the input and outputs of the converter. This phenomenon is used to protect the sensitive loads, the output of the converter can be configured with positive or negative polarity and it has very high noise interference capability (LIU et al., 2017). For the non-isolated DC-DC converters the electrical barrier is supposed to be absent, enabling them to have simple design and reduced cost (RAGHAVENDRA et al., 2019).

However, when converters are supplied by the utility grid, galvanic isolation (high frequency transformer) is necessary for safety reasons: the utility grid can achieve high voltage surges, which can be destructive to loads in non-isolated converters. The isolated power supplies utilize more than one switching converter topology, including Half-bridge, Full-bridge, Dual Half-bridge, Flyback, and Push-pull converters. Even so, the most widely known of these is the Flyback converter, mainly used in low power offline power supply design (power supplies designed to directly accept electric power from an alternating current utility power source), typically less than 150 W (SEMINAR, 2020). Briefly, the Flyback converter is realized when a transformer replaces the inductor of the buck-boost converter (ALATAI et al., 2021).

Accordingly, the Flyback converter transformer combines the actions of an isolating transformer and an output inductor into a single element, while being capable of providing multiple output voltages. In spite of that, for many designers the Flyback topology is synonymous with low performance, low efficiency and poor cross-regulation, so to operate

this topology to its full potential, many small and not obvious subtleties must be well understood (SEMINAR, 2010).

1.1 Motivation and Problematic

An important factor involving the use of Flyback converter for battery recharging is how to implement the CC-CV charging method considering the isolation while maintaining a good cross-regulation between the outputs. Many studies have been presented considering different control strategies to obtain the CC-CV charge, each focusing on different aspects of development, for instance methods to improve efficiency, a power factor correction approach or a more feedback control focused strategy related to CC-CV charging.

The CC-CV charging implementation on a Flyback converter is intimately related with the feedback control loop. As described previously, during CC mode it is necessary to limit the output current through the feedback loop. Also, when the battery is charging, the internal resistance increases and it takes less current, in which case the battery voltage increases to its nominal rate and the feedback has to effectively provide the PWM switcher with the error signal so the CV mode can be implemented (ESHKEVARI; ZARE, 2017a). Thus, there are many ways to control and provide the error signal, so the switcher can regulate its duty cycle. There are topologies that use an auxiliary winding that will regulate the output voltage and current from the primary side, while many others provide the error signal from the output using an optocoupler. They are respectively called primary and secondary side regulation. Accordingly, the control loop and the battery pack characteristics need to be well linked, thus the battery will not be damaged and the charge time can be optimized.

During the last decades, studies and advancements have presented a plethora of flyback development and control methods due to the advantages previously mentioned. For example, (SINGH; CHATURVEDI, 2007) discusses the design and performance of a power factor corrected Flyback converter carried out for low power battery charging applications, operating in discontinuous conduction mode (DCM) and implementing a secondary side feedback approach. However, it does not explicit the CC-CV charging characteristics for fast charging that could be designed alongside the studied converter. On the other hand, (SOUSA et al., 2009) studies a Flyback based battery charger for uninterruptible power systems application, it designs the CC control loop through primary side regulation and the CV feedback network provided by the secondary side with the use of an optocoupler. (KUSHWAHA; SINGH, 2018) focuses on designing a non-isolated bridgeless buck-boost converter for input power factor correction that feeds a Flyback converter to facilitate charging during the CC-CV modes, both implemented using secondary side regulation. In (HOQUE; HANNAN; MOHAMED, 2016) a secondary side regulated proportional-

integral (PI) controller was developed for a charge equalization controller applied to li-ion batteries, the PI controller was designed to control the CC-CV charging and its parameters were modeled using the particle swarm optimization algorithm. Finally, in both (ESHKEVARI; ZARE, 2017b) and (JHA; SINGH, 2021), a Flyback based battery charger was proposed with secondary side controlled CC-CV charging using the quasi-resonant switching approach.

1.2 Contribution and Objectives

Although these and many other studies have provided important aspects for the development of flyback based battery chargers, few have provided a complete description on the modeling of the converter and its control circuit parameters. Futhermore, even less studies describe how the system can be adapted, thus the output voltage can be varied in order to supply the CC-CV strategy to a larger pack of li-ion batteries in series. Thus, this work aims to provide a description of Flyback based battery charger operating in DCM with CC-CV secondary side regulation and variable output voltage. Therefore, this work provides the following contributions:

- Modeling of a DCM Flyback converter;
- Analysis of the resonant effects and how to mitigate them with snubbers;
- Modeling of secondary side control circuit in order to regulate the CC-CV charging profile;
- Analysis and description of a peak current-mode PWM control integrated circuit and how the error signal from the secondary influences the MOSFET switching along with the inductor current;

1.3 Structure

In order to encompass all the objectives introduced. This work is divided into five chapters. In this first chapter was presented the contextualization, motivation, objectives and contributions.

For the other chapters, this work is outlined as follows: Chapter 2 provides a literature review of Flyback in DCM operation, its design necessities and the control system modeling.

Chapter 3 presents the methodology used to implement Flyback converter based charger operating in DCM, how a current PWM controller was used so the system could be studied through the *PLECS* software and the defined parameters for Flyback power

stage and feedback system. The chapter provides a parallel to the separate topics discussed in the Chapter 2.

Chapter 4 presents the results obtained for the proposed system and discusses the main points observed. Finally, conclusions are stated in Chapter 5, as well as proposals for the continuity of this work.

2 Literature Review

In this chapter, a theoretical review of the most relevant concepts, design, control strategy and main components implemented in Flyback converters operating in Discontinuous-Conduction Mode (DCM) characteristics are presented.

2.1 A DCM Flyback Converter

The Flyback converter is based on the buck-boost converter (ERICKSON; MAKSIMOVIC, 2007). Its power electronics stage circuit is illustrated in Figure 3. Basically, it operates by first storing the energy from an input source into the coupled inductor while the primary switch is on. When the switch turns off, the transformer reverses due to the inductor current behavior, forward-biasing the output power diode and delivering the energy to the output (SEMINAR, 2010).

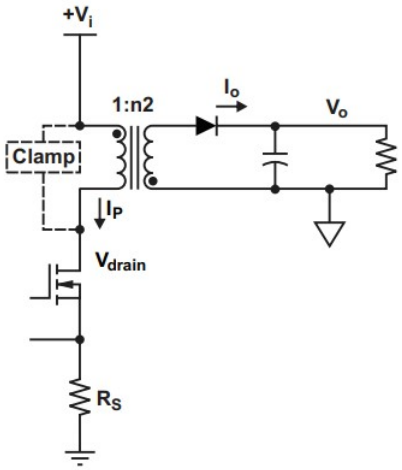

Figure 3 – Flyback power electronics main circuit. From: (SEMINAR, 2010).

Flyback converters have two main modes of operation: Continuous-Conduction Mode (CCM) and Discontinuous-Conduction mode (DCM). The topology is chosen given the necessities of the design: cost, size, components specifications, frequency of operation, efficiency and many others. For many low-power and low-current applications, however, the DCM Flyback converter can provide a more compact and low-cost option. The current in the indcutor behavior when operating in DCM results in lower inductance value, which directly relates to its size and price. Although there are disadvantages for the DCM operation, such as its impact on the efficiency due the higher RMS current in the inductor, higher peak rectifier current, increased input and output capacitance, the impact on cost and size greatly weights the decision when it is applied to low-power converters

(SEMINAR, 2010; SEMINAR, 2020; BETTEN, 2020). In addition to the transformer size and price, there are several other advantages for DCM Flyback converters (SEMINAR, 2010; BETTEN, 2020):

- No diode recovery loss
- Minimal FET turn on losses
- No right half plane zero control issues
- Slope compensation is not required

The main aspect of the DCM Flyback is that all of the energy stored in the transformer is transferred to the load during the off period. In other words, the power diode current decreases to zero before the start of next switching cycle. Thus, decreasing the current to zero before switching will reduce dissipation in the field-effect transistor (FET) and reduce rectifier losses, and will often reduce the coupled inductor size requirement as well (BETTEN, 2020). Figure 4 shows the key components switching waveforms, where D is the duty cycle, T_s is the switching period, V_o is the output voltage, V_i is the input voltage, n_2 is the number of turns on secondary side inductor, I_{pk} is the peak current value through the primary side inductor, and I_{o-avg} is the average secondary current. Fundamentally, operation starts when the power MOSFET turns on for the period DT_s, when the current on the primary side winding reaches its peak set by the primary winding inductance, the input voltage, the on-time and the control circuit which will be further described later in this chapter. During this period the secondary side diode is reversed biased due the secondary winding polarity, so that all the output current is supplied by the output capacitor.

The second mode occurs during the $(1 - D)T_s$ period of T_s, when the MOSFET turns off. In this case, the transformer polarity is reversed and the diode is forward biased, which allows it to conduct current to the load and recharge the capacitor. The current through the diode I_o will decrease linearly from its peak to zero, where it remains until the next switching cycle (idle period). After all the energy once stored in the transformer is depleted, only residual ringing remains during the idle period (BETTEN, 2020; SEMINAR, 2010).

The development of a DCM flyback begins with the selection of the switching frequency (f_{sw}), a maximum desired duty cycle (D_{max}), and an estimated target efficiency, (η). Thus, the maximum on time is given by Equation (2.1).

$$t_{on_{max}} = \frac{D_{max}}{f_{sw}}. \tag{2.1}$$

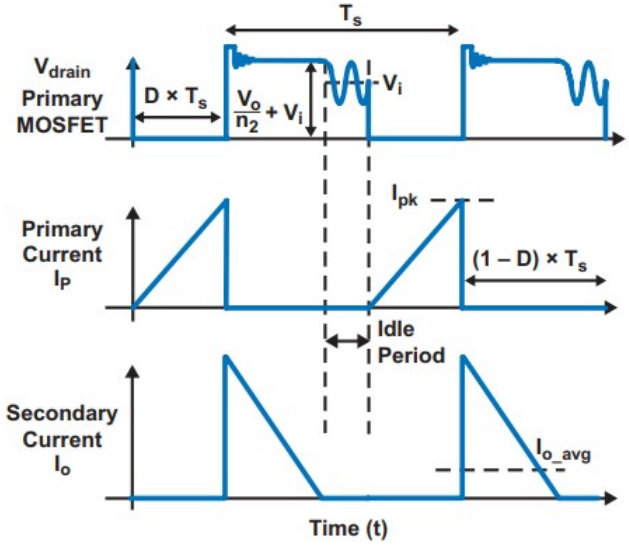

Figure 4 – DCM operation waveforms. From: (SEMINAR, 2010).

Defining $V_{ds_{on}}$ as the voltage across the MOSFET while it is conducting, V_{RS} as the current sense resistor (R_S in Figure 3) voltage, $V_{in_{min}}$ as the minimum input voltage and $P_{o_{max}}$ as the maximum output power, the maximum transformer's peak primary current can be estimated by (BETTEN, 2020):

$$I_{pk} = \frac{P_{o_{max}} \cdot 2/D_{max}}{(V_{in_{min}} - V_{ds_{on}} - V_{RS}) \cdot \eta}. \tag{2.2}$$

The required relationship between the number of turns for the transformer windings can by achieved by the relationship between the energy stored and depleted during the on and off time of the MOSFET, respectively. In other words, the voltage relationship during the conduction time of each winding during a switching cycle, as shown in Equation (2.3). Where x is a minimum desired idle time and V_d is the forward biased voltage across the diode (BETTEN, 2020).

$$\frac{N_p}{N_s} = \frac{(V_{in_{min}} - V_{ds_{on}} - V_{RS})t_{on_{max}}}{(\frac{1}{fsw}(1-x) - t_{on_{max}})(V_o - V_d)}. \tag{2.3}$$

Two other important parameters to be aware of are the *flat-top* voltages across the MOSFET and the output diode, so the components can be chosen accordingly in respect to their breakdown voltages. Therefore, Equation (2.4) and Equation (2.5) define the *flat-top* voltages across the MOSFET and diode, respectively. Note $V_{ds_{max}}$ is defined by the input voltage and the secondary side winding voltage reflected on the primary. Similarly, the maximum peak inverse voltage across the diode is determined by the output voltage and the maximum input voltage reflected on the secondary side winding. It can be observed in Figure 4 that the MOSFET, and consequently, the diode have ringing due to the transformer leakage inductance (as will be explained in Section 2.2), it is

recommended to expect the actual value to be $10-30\%$ higher than predicted (SEMINAR, 2010; BETTEN, 2020). Equations (2.4) to (2.11) are developed and described in depth in (BETTEN, 2020).

$$V_{ds_{max}} = V_{in_{max}} + (V_o + V_d)\frac{N_p}{N_s}. \tag{2.4}$$

$$V_{piv_{max}} = V_o + \frac{V_{in_{max}}}{\frac{N_p}{N_s}}. \tag{2.5}$$

The maximum on time can be better estimated now with Equation (2.6), although it should not be very different from the one found in Equation (2.1).

$$t_{on_{max}} = \frac{(V_o + V_d)(\frac{1}{fsw}(1-x))\frac{N_p}{N_s}}{V_{in_{min}} + (V_o + V_d)\frac{N_p}{N_s}}. \tag{2.6}$$

Thus, the maximum required primary side inductance is given by:

$$L_{pmax} = \frac{V_{in_{min}}^2 \cdot t_{on_{max}}^2 \cdot \eta f_{sw}}{2 \cdot V_o \cdot I_{o_{max}}}. \tag{2.7}$$

where $I_{o_{max}}$ is the maximum average output current. The maximum duty cycle can be now calculated with Equation (2.8), where L_p is the primary side inductance chosen value.

$$D_{max} = \frac{2 f_{sw} V_o I_{o_{max}} L_p}{\eta V_{in_{min}}^2}. \tag{2.8}$$

Therefore, the maximum primary side peak current I_{pk} and and its maximum root-mean-square (RMS) can be found using Equations (2.9) and (2.10), respectively.

$$I_{pk_{max}} = \sqrt{\frac{2 V_o I_{o_{max}}}{\eta L_p f_{sw}}}. \tag{2.9}$$

$$I_{pk_{rms}} = I_{pk_{max}} \sqrt{D_{max}/3}. \tag{2.10}$$

The maximum current-sense resistor value allowed is based on the on the selected controller's current-sense input minimum current limit threshold, V_{cs}, and can be determined simply by:

$$R_{RS_{max}} = \frac{V_{cs}}{I_{pk_{max}}}. \tag{2.11}$$

Finally, the output and input (normally after the bridge rectifier) capacitor are considered. The output capacitor is generally selected as larger than that of Equation (2.12), which is based on the maximum output voltage ripple (ΔV_o) and its equivalent

series resistor (R_{esr}). The minimum required input capacitor is also a function of the input bus voltage ripple ΔV_{in}, and is defined by Equation (2.13) (BETTEN, 2020).

$$C_o = \frac{I_{o_{max}}(1-D)}{(\Delta V_o - I_{pk}\frac{N_p}{N_s}R_{esr})f_{sw}}. \tag{2.12}$$

$$C_{inmin} = \frac{I_{pk}D}{2\Delta V_{in}f_{sw}}, \tag{2.13}$$

where D is the expected steady-state duty cycle given by Equation (2.14) (BASSO, 2014), where R_o is the operating load resistance.

$$D = \frac{V_o}{V_{in}}\sqrt{\frac{2L_p f_{sw}}{R_o}}. \tag{2.14}$$

2.2 Snubber Circuits

Previously, the transformer and all other components were considered ideal for simplicity of explanation. However, this is not true for real-life applications. The coupled inductor has its parasitic components: the leakage inductance L_{Lk} and the and the primary winding capacitance C_{prim}. Furthermore, the switching MOSFET has an inherent output capacitance C_{oss} between the drain and source terminals. In Figure 5 is represented a basic Flyback structure including their major parasitic components. The MOSFET output capacitance in combination with the leakage inductance and the winding capacitance have a remarkable impact on the performance of the converter (SONST, 2021).

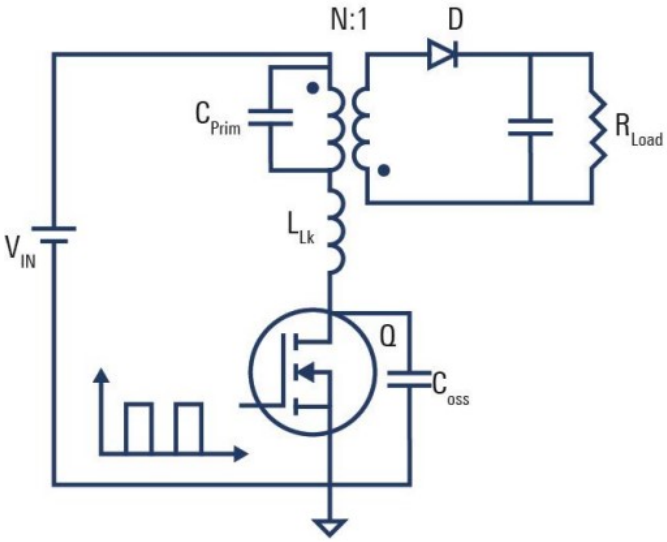

Figure 5 – Flyback structure with parasitic components. From: (SONST, 2021).

The primary leakage inductance L_{Lk} does not take part in the energy transfer from primary to secondary as does the magnetizing inductance L_m. The energy stored in the L_{Lk} is lost and generates a voltage spike at the beginning of the turn-off time at the drain terminal of the MOSFET. Figure 6 shows the resonant effects of the parasitic components. The high voltage spike described is visible. The effectiveness of the damping effect is not very high in this resonant circuit, represented by the oscillation, typically in the frequency range of several MHz, last for several periods which is undesired for it can degrade EMI performance (RIDLEY, 2005; SONST, 2021).

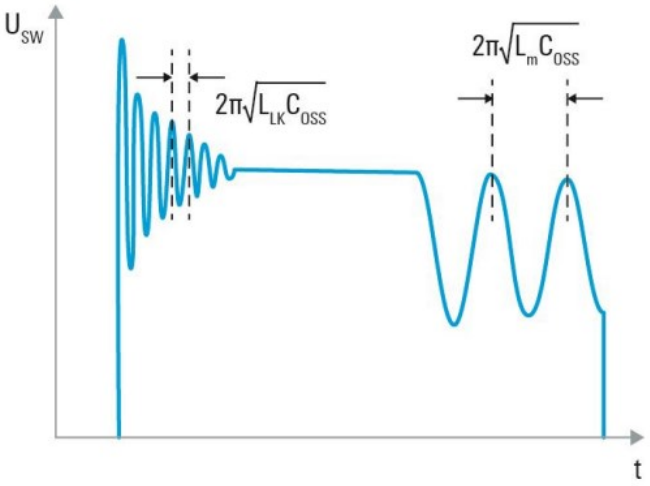

Figure 6 – Switch node voltage waveform. From: (SONST, 2021).

The resonance that takes place during the idle period is also visible in Fig. 6. It occurs after all energy is depleted, so it is determined by magnetizing inductance L_m and the capacitance C_{oss} and therefore the frequency is much lower.

The main issue caused by these resonant combinations is when the high voltage spike ($V_{ds_{peak}}$) created by the switch-off mechanism is not properly clamped or damped. The maximum breakdown voltage of the MOSFET may be exceeded and the transistor might be destroyed. The peak voltage at the switch is given by Equation (2.15), where L_{Lk} is normally 1% to 15% of L_p (WOODING; BEER, 2011; SCHLESINGER; BIELA, 2019). Hence, snubbers have to be considered when designing a flyback converter to clamp voltage spikes and damp high frequencies in order to avoid unwanted situations (SEMINAR, 2010; SONST, 2021).

$$V_{ds_{peak}} = I_{pk}\sqrt{\frac{L_{Lk}}{C_{prim} + C_{oss}}} + V_{in} + V_o\frac{N_p}{N_s}. \tag{2.15}$$

Overall, snubbers are circuits placed across semiconductor devices or transformers for protection purposes and to improve performance. Snubbers can reduce or even eliminate

voltage or current spikes, limit dI/dt or dV/dt and can also reduce EMI by damping the voltage and current ringing. There are many different kinds of snubbers, however there are two commonly used ones, the resistor-capacitor (RC) damping network and the resistor-capacitor-diode (RCD) turn-off snubber circuit.

2.2.1 Flyback Snubber Design

Applying snubbers to a Flyback converter is essential to obtain a reliable design. They can be designed as either passive or active circuit. The passive snubber circuits components are restricted to capacitors, inductors and diodes, and they can be dissipative or non-dissipative systems. If the energy in the snubber is dissipated in a resistive element, it is classified as a dissipative snubber. Two dissapitive snubber topologies will be discussed here: the resistor-capacitor-diode (RCD) and the resistor-capacitor (RC) damping network.

2.2.1.1 The Primary RCD-Snubber Circuit

This topology consists of a diode in series with capacitor-resistor parallel association. As shown Figure 7, it is placed in parallel with coupled the inductor primary side.

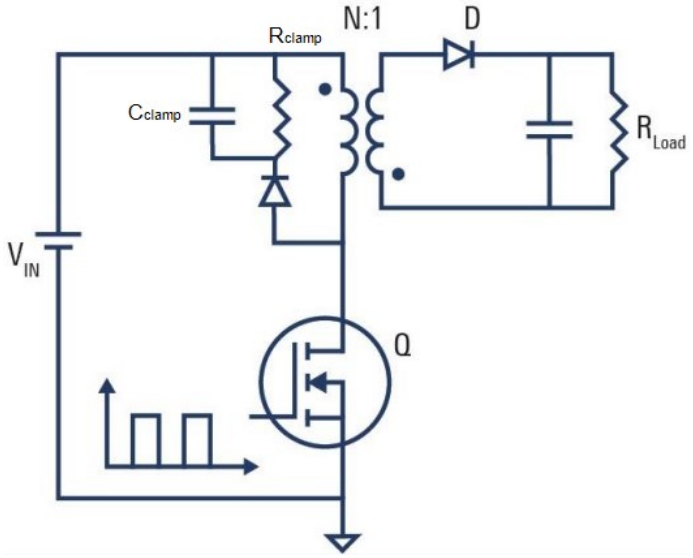

Figure 7 – Flyback structure with a RCD snubber. From: (SONST, 2021).

It belongs to the class of the dissipative snubber and absorbs the energy stored in the leakage inductance in two steps. Initially, the current generated by L_{Lk} flows into the capacitor when MOSFET drain voltage is above the clamping voltage. Afterwards, the resistor discharges the clamping capacitor and dissipates the energy into heat. This method is simple and relatively inexpensive, but the fact that the energy is dissipated into heat reduces the converter efficiency, and the power loss increases with the switching frequency (SONST, 2021).

The value of the snubber resistor is given by Equation (2.16).

$$R_{clamp} = \frac{2V_{clamp}(V_{clamp} - V_o\frac{N_p}{N_s})}{L_{Lk}f_{sw}I_{prim}^2}, \tag{2.16}$$

where $V_{clamp} = V_{Lk} + V_o(N_p/N_s)$, and V_{Lk} is the voltage across the leakage inductance.

The value of the clamp capacitor is not critical and depends on how much ripple voltage (ΔV_{clamp}) the design can tolerate:

$$C_{clamp} = \frac{V_{clamp}}{\Delta V_{clamp}f_{sw}R_{snubber}}. \tag{2.17}$$

The snubber capacitor should be a ceramic capacitor or another material that offers low ESR at higher frequency, so it can provide an impedance curve which fits to the application (SONST, 2021).

2.2.1.2 The primary RC-Damping circuit

After the reverse recovery period of the RDC-snubber clamp diode is completed, the primary is unclamped and the L_{Lk} will ring with the C_{oss} of the main switch. It is important to mention that the RDC-clamp does not eliminate all primary circuit ringing, therefore an additional snubber circuit is beneficial in order to optimize EMI emissions (SONST, 2021). This resonant effect after the diode reverse recovery can be minimized with the use of the RC-Damping circuit connected at switch node, as illustrated in Figure 8.

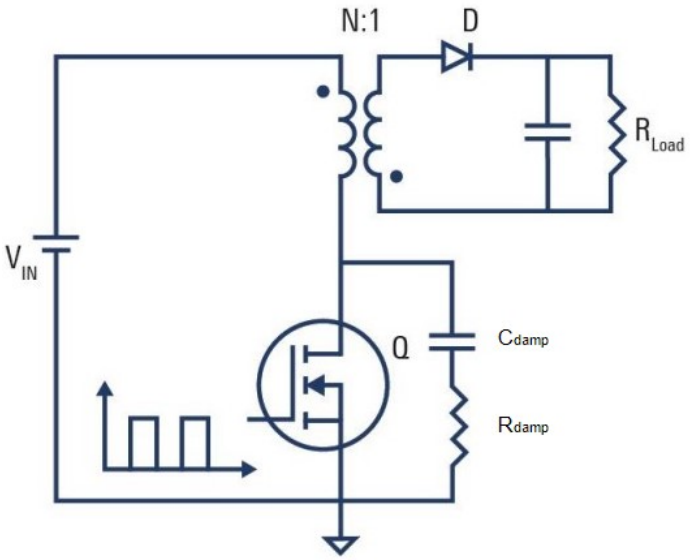

Figure 8 – Flyback structure with a RC snubber. From: (SONST, 2021).

The parameters of this damping circuit depend on the resonant frequency between L_{Lk} and C_{oss}, given by $f_r = 1/(2\pi\sqrt{L_{Lk}C_{oss}})$. Thus, the resistor R_{damp} and capacitor

C_{damp} can be respectively determined by Equations (2.18) and (2.19) (RIDLEY, 2005).

$$R_{damp} = 2\pi f_r L_{Lk}. \tag{2.18}$$

$$C_{damp} = \frac{1}{2\pi f_r R_{damp}}. \tag{2.19}$$

2.3 Control System

For the Flyback and other switching converters, the desired output voltage $v(t)$ is a function of the input line voltage $v_g(t)$, the duty cycle $d(t)$, the load current $i_{load}(t)$, and the values of the circuit components. The most important objective of dc-dc converter controllers is to maintain a constant output voltage $v(t) = V$, or the controlled variable (sometimes the output current is the variable to be controlled), even when submitted to disturbances in $v_g(t)$ and $i_{load}(t)$ and other variations in the converter circuit elements. Figure 9 shows a typical situation, where the sources of variations or disturbances for $v_g(t)$ and $i_{load}(t)$ are diverse. The input voltage, $v_g(t)$, may typically contain periodic variations at the second harmonic of the ac power system frequency, due to the bus capacitor normally placed after the bridge rectifier. Considering as well that the utility grid is supplying other circuits and systems, $v_g(t)$ magnitude might vary when the other power system loads are switched on or off, or when there are abnormalities in the electric distribution power system. Furthermore, the load current $i_{load}(t)$ is variable in many systems, and these variations can be instantaneous or slow, which might also impact on the robustness of the converter. Consequently, it is desired to have the output voltage limited to a specified range, but this is not practical to achieve without the use of negative feedback (MITCHELL; MAMMANO, 2001; ERICKSON; MAKSIMOVIC, 2007)

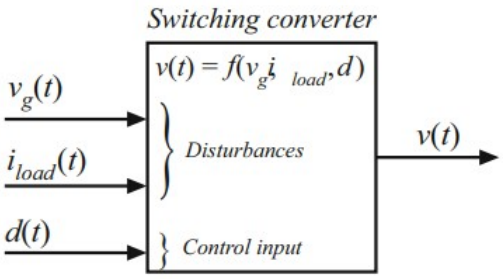

Figure 9 – Functional block diagram illustrating the dependencies of $v(t)$. From: (ERICKSON; MAKSIMOVIC, 2007).

Although the equations that define the input-output steady-state relationship of a switching converter might imply that a duty cycle will give an exact output value, such as Equation (2.14), these equations do not account for the system's reaction to disturbances. Therefore, when designing negative feedback the purpose is to build a circuit that regulates

the necessary duty cycle, obtaining the desired output voltage in spite of the variations previously mentioned (ERICKSON; MAKSIMOVIC, 2007; WANG, 2014).

Figure 10 shows a block diagram for the feedback system. Basically, the output voltage $v(s)$ is measured using a voltage sensor with a gain, most of the times a voltage divider comprised of precision resistors. The sensor output signal is then compared with a reference input voltage v_{ref}. The difference between them is called the error signal, designated as $v_e(s)$. The error signal is usually nonzero but small nevertheless. Hence, one of the goals when adding a compensator network is to obtain a small error. The transfer function from the error signal $v_e(s)$ to the output voltage $v(s)$ is equal to the gains of the compensator, pulse-width modulator, and the converter power stage. If the compensator gain is large enough in magnitude, then a small error signal can produce the required output voltage $v(t) = V$ for a dc regulator (ERICKSON; MAKSIMOVIC, 2007). So the complete system must designed in order to ensure stability and a controlled output.

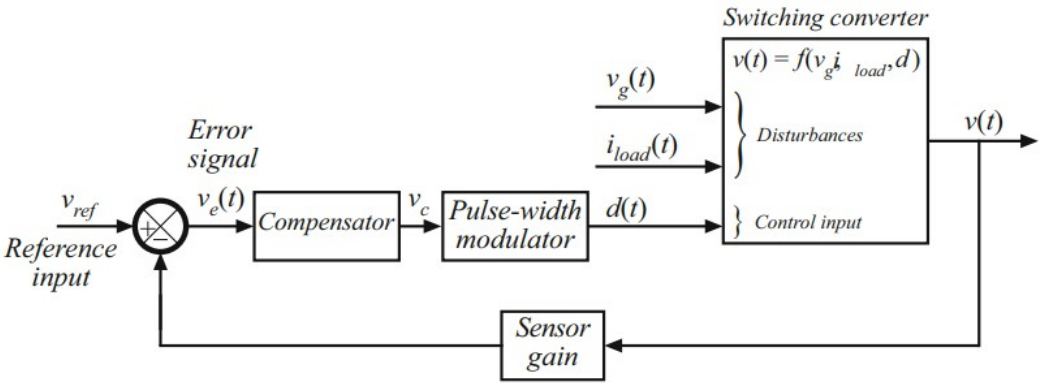

Figure 10 – Negative feedback control system for switching converters block diagram. From: (ERICKSON; MAKSIMOVIC, 2007).

It is important, however, before studying how to designed the compensator network to avoid any unstable effects, to understand how the pulse-width-modulator (PWM) block works and how the duty cycle is generated from the compensator output v_c.

2.3.1 Peak Current mode PWM Control

The peak current mode control (PCMC) is often the preferred PWM method when designing low power isolated power supplies using Flyback converters (CHEN, 2014). Basically, it compares the peak current over the power MOSFET of the Flyback through a shunt resistor with the compensated error signal to define the duty cycle. The fundamental circuit and DCM waveform are shown in Figure 11. Therefore, it can be noted that the frequency clock sets an RS flip-flop, which tuns on the power MOSFET, causing the current through the inductor i_L to ramp up. When the sensed inductor current, $v_s = R_s i_L$ (R_s being the shunt resistance), is equal to v_c, the compensated error signal, the power

MOSFET is turned off and i_L starts to ramp down. If the converter is operating with $d > 0.5$, V_{ramp} will be needed to prevent potential instability. In Figure 11, S_e, S_n and S_f are the slope of V_{ramp}, the slop of i_L during the power MOSFET's turn on, and the slop of i_L during the power MOSFET's turn off, respectively (MITCHELL; MAMMANO, 2001; KLEEBCHAMPEE; BUNLAKSANANUSORN, 2005).

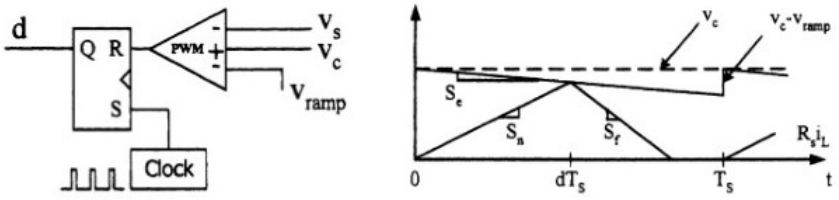

Figure 11 – Peak current mode control operation. From: (KLEEBCHAMPEE; BUNLAKSANANUSORN, 2005).

2.3.2 Stability

The main aspect of designing control loops for switching converters is how to provide the compensated signal v_c and ensure the system's stability. Figure 12 shows the control system block diagram derived from Figure 10, which a loop gain transfer function can be derived as Equation (2.20), defined as the product of the gains around the forward and feedback paths (ERICKSON; MAKSIMOVIC, 2007). Each block has its own transfer function, which depends not only on the type of converter used, but also on the components and IC's implemented in the project (MITCHELL; MAMMANO, 2001; KLEEBCHAMPEE; BUNLAKSANANUSORN, 2005; ERICKSON; MAKSIMOVIC, 2007). For instance, the value of V_m, located in the PWM modulator block, will be determined by the circuits inside the integrated circuit, as well as $G_{vd}(s)$ will depend on the converter topology chosen and also the type of conduction mode implemented. Since the discussion in this section encompass converter control in general, the equation for $G_{vd}(s)$ for a DCM Flyback converter will be presented and analyzed in the next chapter.

$$G(s) = H(s)G_c(s)G_{vd}(s)/V_m. \tag{2.20}$$

It is necessary to consider that the closed loop transfer function might contain right half-plane poles, even when the transfer function of the original converter $G_{vd}(s)$, which depends on the converter topology chosen, as well as of the loop gain $G(s)$, do not contain right half-plane poles. When that happens the feedback loop regulation would not operate accordingly and oscillations are usually observed. Also, even if the feedback

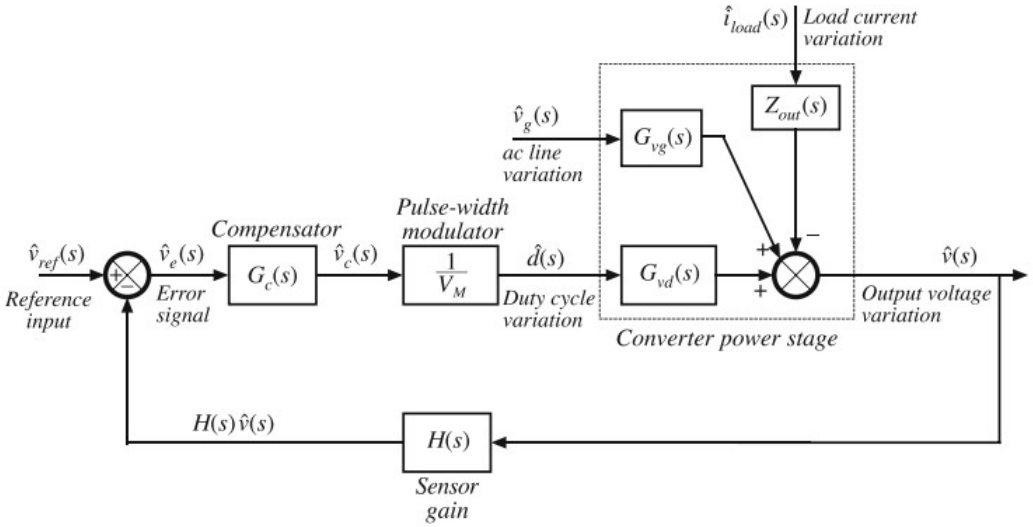

Figure 12 – Switching converter control system. From: (ERICKSON; MAKSIMOVIC, 2007).

system is stable, it is possible for the transient response to exhibit undesirable ringing and overshoot (ERICKSON; MAKSIMOVIC, 2007; BASSO, 2014).

The closed loop transfer function, when using negative feedback, is then given by Equation (2.21). Hence, this equation needs to be evaluated in regards to stability. In other words, the presence of roots in the right half-plane in the denominator $1 + G(s)$ needs to be evaluated.

$$\frac{G(s)}{1 + G(s)}. \tag{2.21}$$

There are many methods of studying the stability of a transfer function. The function resulted from the denominator of Equation (2.21) could be factored and checked if any of the roots have positive real parts. While this method can provide the necessary evaluation, it results from an unnecessary effort. The phase margin test, derived from the Nyquist stability theorem, is sufficient for designing most voltage regulators (ERICKSON; MAKSIMOVIC, 2007).

The phase margin test evaluates the loop gain phase response at the crossover frequency. Given by f_c, the crossover frequency is the frequency with which the magnitude of the loop gain is unity, or

$$||G(2\pi f_c)|| = 1 \Rightarrow 0\ dB. \tag{2.22}$$

The phase margin ϕ_m is then calculated by evaluating the phase of the loop gain at the crossover frequency and adding 180°. Stability is indicated when the phase margin

is positive and recommended to be above 45°, as shown in Equation (2.23) (MITCHELL; MAMMANO, 2001; ERICKSON; MAKSIMOVIC, 2007).

$$\phi_m = 180° + \angle G(j2\pi f_c) > 45°. \tag{2.23}$$

2.3.3 Regulator Design

In order to design a Flyback feedback control loop, it is necessary to design a circuit that can provide the error signal from the secondary side to primary side while providing the compensated v_c. The majority of consumer power supplies involve a TL431 placed on the isolated secondary side to feed the error back to the primary side via an optocoupler (BASSO, 2012). This combination provides a method of designing the compensator control block $G_c(s)$ to ensure stability and a desired response.

2.3.3.1 TL431-Based Compensators

The TL431 has an equivalent structure shown in Figure 13. Basically, it combines an open-collector op amp with a precise 2.5 V reference voltage, so that when the voltage over the reference pin R exceeds the internal reference level, the bipolar transitor starts to conduct and a current is sunk between the cathode and anode pins. Being an active element, it needs a minimum voltage to operate and a certain quantity of consumed current as well. Hence, the supply voltage cannot be lower than 2.5 V across the cathode and anode of the component, and the bias current must be set to at least 1 mA (BASSO, 2014).

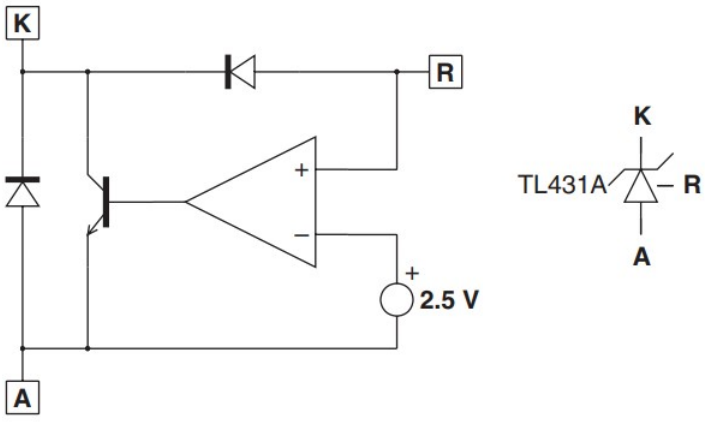

Figure 13 – TL431 equivalent structure. From: (BASSO, 2014).

The device can be considered as a trasnconductance amplifier: in classical loop-control structure, the TL431 observes a fraction of the output voltage seen by its reference pin and converts it into an output current sunk between the cathode and the anode (BASSO, 2012).

A common method of structuring the TL431 with the feedback circuitry is shown in Figure 14, this and others compensator networks are deeply discussed in (BASSO, 2012).

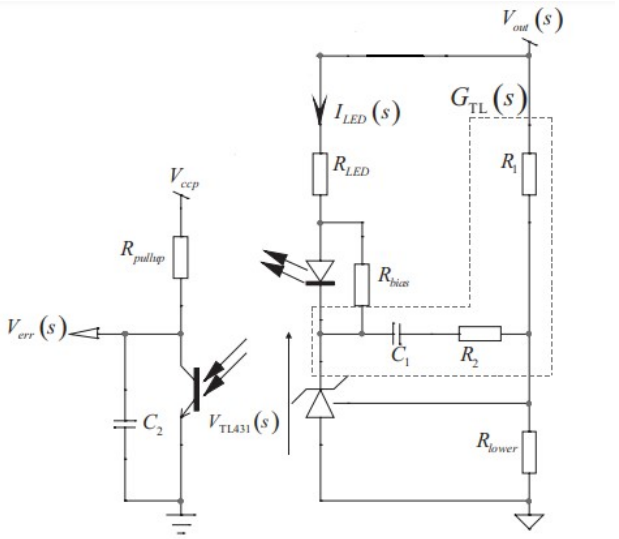

Figure 14 – A TL431-based feedback network. Adapted from: (BASSO, 2012).

The controller $G_c(s)$ is designed by structuring it for the desired DC and AC response of the system. For the DC response, first the voltage divider R_1 and R_{lower} (the current through the TL431 reference pin is very small so it behaves as a voltage divider) has to be a combination that with $V_{ref} = 2.5\ V$ across R_{lower}, V_{out} will be the desired output voltage (SCHÖNBERGER, 2013). Hence,

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_{lower}}\right). \tag{2.24}$$

Also, the TL431 requires a minimum current to operate in favorable conditions. Furthermore, it needs a minimum voltage to deliver its performance, which is equal to the internal reference value and cannot be lower than $2.5\ V$. Figure 14 shows a typical arrangement where the optocoupler collector pulls the feedback pin down as the LED current increases. R_{LED} limits the maximum LED current. However, the TL431 has biasing conditions with respect to the minimum current of $1\ mA$ at least and the minimum operating voltage, which creates an upper limit to R_{LED}. Thus, in order to establish the $R_{LED_{max}}$, it is necessary to analyze the situation which the current through the optocoupler output is maximum and brings the feedback voltage close to ground. In other words, when the transistor reaches its saturation voltage, $V_{CE_{sat}}$. Therefore,

$$I_{C_{max}} = \frac{V_{cc} - V_{CE_{sat}}}{R_{pullup}}. \tag{2.25}$$

The current flowing through the collector to emitter needs the photons emitted by the internal LED and collected by the transistor base area. The relationship between the

collector current I_C and the LED current I_F is defined by the current transfer ratio (CTR). Normally, the CTR has a typical value given by the specific datasheet, but it can vary within a specified range. So in order to cover unavoidable dispersions, it is necessary to use the minimum value of this CTR parameter. From figure 14, the current flowing through R_{LED} also includes the additional bias current brought by R_{bias} (used to provide the TL431 with the minimum biasing current of 1 mA). Hence, the $I_{R_{LED_{max}}}$ can be determined:

$$I_{R_{LED_{max}}} = \frac{I_{C_{max}}}{CTR_{min}} + I_{bias} = \frac{V_{cc} - V_{CE_{sat}} + I_{bias}R_{pullup}CTR_{min}}{R_{pullup}CTR_{min}}. \tag{2.26}$$

The LED current depends not only on the output voltage, but also on the forward drop of the diode itself and the minimum operating voltage acceptable for the TL431. Thus, from Figure 14, the maximum R_{LED} current is also given by

$$I_{R_{LED_{max}}} = \frac{V_{out} - V_f - V_{TL431_{min}}}{R_{LED}}. \tag{2.27}$$

Therefore, by equating (2.26) and (2.27) and solving for $R_{LED,max}$, it is determined the value from which the R_{led} cannot not exceed:

$$R_{LED_{max}} \leq \frac{V_{out} - V_f - V_{TL431_{min}}}{V_{cc} - V_{CE_{sat}} + I_{bias}CTR_{min}R_{pullup}} R_{pullup}CTR_{min}. \tag{2.28}$$

Henceforth, the DC operating point conditions fix the upper excursion of the value of the LED series resistor (BASSO, 2012).

When it comes to the AC analysis, or the frequency response, the $G_c(s)$ controller is designed considering the small signal variations, so its transfer function can be defined to ensure stability and acceptable response to variations of $v_g(t)$ and $i_{load}(t)$. Thus, in order to define the transfer function $G_c(s) = V_{err}(s)/V_{out}(s)$, the TL431 network is analyzed in the frequency domain. In this case, the reference voltage of the TL431 is constant, $V_{ref}(s) = 0$, and the voltage $V_{TL431}(s)$, given by Equation (2.29), is determined by the device's amp op characteristics, as shown in Figure 13.

$$V_{TL431}(s) = -V_{out}(s)\frac{R_2 + \frac{1}{sC_1}}{R_1} = -V_{out}(s)\frac{sR_2C_1 + 1}{sR_1C_1}. \tag{2.29}$$

Then, it is simple to derive the AC current through the LED:

$$\begin{aligned} I_{LED}(s) &= \frac{V_{out} - V_{TL431(s)}}{R_{LED}} = \frac{V_{out}}{R_{LED}}\left(1 + \frac{sR_2C_1 + 1}{sR_1C_1}\right) \\ &= V_{out}\frac{1}{R_{LED}}\left[\frac{s(R_1 + R_2)C_1 + 1}{sR_1C_1}\right]. \end{aligned} \tag{2.30}$$

For the AC analysis, this current multiplied by the CTR is the optocoupler transistor's current. Considering the voltage feeding the collector through the pull up resistor is constant and, therefore, $V_{cc}(s) = 0$, the AC circuit is basically the V_{err} as the node with R_{pullup} in parallel with the transistor and the capacitor C_2. Hence,

$$V_{err}(s) = -I_{LED}(s)CTR\frac{R_{pullup}\frac{1}{sC_2}}{R_{pullup}+\frac{1}{sC_2}} = -I_{LED}(s)CTRR_{pullup}\frac{1}{1+sR_{pullup}C_2}. \tag{2.31}$$

As a consequence, the complete $G_c(s)$ transfer function will given by Equation (2.32).

$$G_c(s) = \frac{V_{err}(s)}{V_{out}(s)} = -CTR\frac{R_{pullup}}{R_{LED}}\frac{1+s(R_1+R_2)C_1}{sR_1C_1(1+sR_{pullup}C_2)}. \tag{2.32}$$

The transfer function above can be put into the normalized form in Equation (2.33) by factoring $s(R_2+R_1)C_1$.

$$G_c(s) = -CTR\frac{R_{pullup}}{R_{LED}}\frac{R_2+R_1}{R_1}\frac{1+1/s(R_1+R_2)C_1}{1+sR_{pullup}C_2} = -G_0\frac{1+\omega_z/s}{1+s/\omega_p}, \tag{2.33}$$

where

$$G_0 = CTR\frac{R_{pullup}}{R_{LED}}\frac{R_2+R_1}{R_1}, \tag{2.34}$$

$$\omega_z = \frac{1}{(R_1+R_2)C_1}, \tag{2.35}$$

and

$$\omega_p = \frac{1}{R_{pullup}C_2}. \tag{2.36}$$

The Equations (2.32) to (2.36) define type 2 controller, which is similar to proportional-integral (PI) controller at low frequencies, with a pole at 0° due to the integral action, and a zero at ω_z due the proportional action. Nevertheless, the type two controller includes a high frequency pole at ω_p, which is used to mitigate the switching ripple (BASSO, 2012; SCHÖNBERGER, 2013; ERICKSON; MAKSIMOVIC, 2007).

3 Methodology

In this chapter, the methodology used to model and design the Flyback power stage and its control parameters for battery charging will be presented. Moreover, the circuit parameters will be established based on the theoretical review presented in Chapter 2 as a means to justify the results discussed in the next chapter.

3.1 Load Definition and Battery Specifications

DC-DC converters are designed based on the load they are supposed to supply. This project aims to provide the CC-CV charging profile for the NCR18650B battery from *Panasonic* (SANYO ENERGY (U.S.A.) CORPORATION, 2012) connected in series. Many combinations of battery packs can be achieved by combining them in series in order to supply higher voltages to different loads. Since the NCR18650B cell has its nominal voltage of 3.6 V and the full charged voltage of 4.2 V, the combinations of battery packs and full charged voltages this project will be designed to supply is given in Table 1.

Table 1 – Quantity of in series connected cells and the respective pack full charged voltage.

Quantity	Full Charged Voltage
3	12.6 V
4	16.8 V
5	21.0 V

Moreover, the maximum current a individual cell can tolerate is 1.625 A. Therefore, the power stage for the flyback converter will be designed for the maximum possible output power, which is for the combination of 5 batteries in series ($V_o = 21$ V) and the maximum cell current, of 1.625 A.

3.2 Flyback Power Stage

According to the discussion presented in Section 2.1, in order to determine the parameters to obtain a DCM operating Flyback converter, it is necessary to define the fundamental working values such as the input voltage range, switching frequency, maximum duty cycle and maximum output voltage and current. Hence, Table 2 shows the predefined values for the project.

Therefore, the parameters from Table 2 can then be applied to the equations presented in Section 2.1 to obtain the values for the power stage circuit. From these calculations it is possible to obtain the best parameters values in order to design a Flyback

Table 2 – Predefined values for the Flyback power stage.

Parameter	Value
Minimum input voltage, V_{inmin}	100 V_{rms}
Maximum input voltage, V_{inmax}	240 V_{rms}
Switching frequency, f_{sw}	50 kHz
Maximum duty cycle, D_{max}	0.45
Output voltage, V_{out}	21 V
Output current, I_{out}	1.625 A
Output voltage ripple, ΔV_{out}	0.2 V

converter operating in Discontinuous-Conduction Mode (DCM). Henceforth, after equating the predefined parameters into them, the chosen values for the converter circuit were gathered and is presented in Table 3.

Table 3 – Circuit values obtained for the desired converter.

Circuit Element	Value
Transformer's winding relation, N_p/N_s	8.4
Transformer's magnetizing inductance, $L_p = L_m$	1 mH
Current sense resistor, R_{sense}	0.2 Ω
Input capacitance, C_{in}	22 μF
Output capacitance, C_{out}	220 μF

It is important to mention that this first study will not be used to create a prototype, so that the values for the MOSFET and secondary side diode voltages when conducting were assumed to be $V_{dson} = V_d = 0.5\ V$ when applied to the equations described in Chapter 2. These values were not based in any particular device and the assumption is based on common values for forward biased voltages accros power transistors and diodes (HART; HART, 2011). Also, according to (SCHLESINGER; BIELA, 2019; WOODING; BEER, 2011), the leakage inductance value for the coupled inductor depends on many transformer specifications such as distance between the windings and core type and can vary between 1-15% of the magnetizing inductance. For this analysis, the leakage inductance was defined 2% of the magnetizing inductance, or $L_{Lk} = 0.02 \cdot L_m = 0.02 \cdot 1\ mH = 20\ \mu H$.

3.3 Snubbers Design

As mentioned previously, the design takes into consideration the leakage inductance for the coupled inductor in order to simulate and analyze the system as close to reality as possible. Also, a capacitance of $C_{oss} = 75$ pF was assumed between the MOSFET's drain and source terminals. However, when these elements are taken into consideration, the ringing and voltages spikes over the MOSFET's terminals when it is switched off should be

expected. Therefore, according to Section 2.2, the RCD and RC, clamping and damping, snubber circuits were determined in order to reduce voltage spikes and attenuate resonant effects, respectively.

Thus, the equations presented in Sections 2.2.1.1 and 2.2.1.2 were then applied to design to obtain the values given in Table 4 for the RCD and RC snubber parameters.

Table 4 – Snubber clamping and damping circuit parameters.

Element	Value
R_{clamp}	65.1 $k\Omega$
C_{clamp}	75 nF
R_{damp}	517 Ω
C_{damp}	75 pF

Henceforth, the open loop flyback circuit designed for the power stage and snubber circuits is shown in Figure 15.

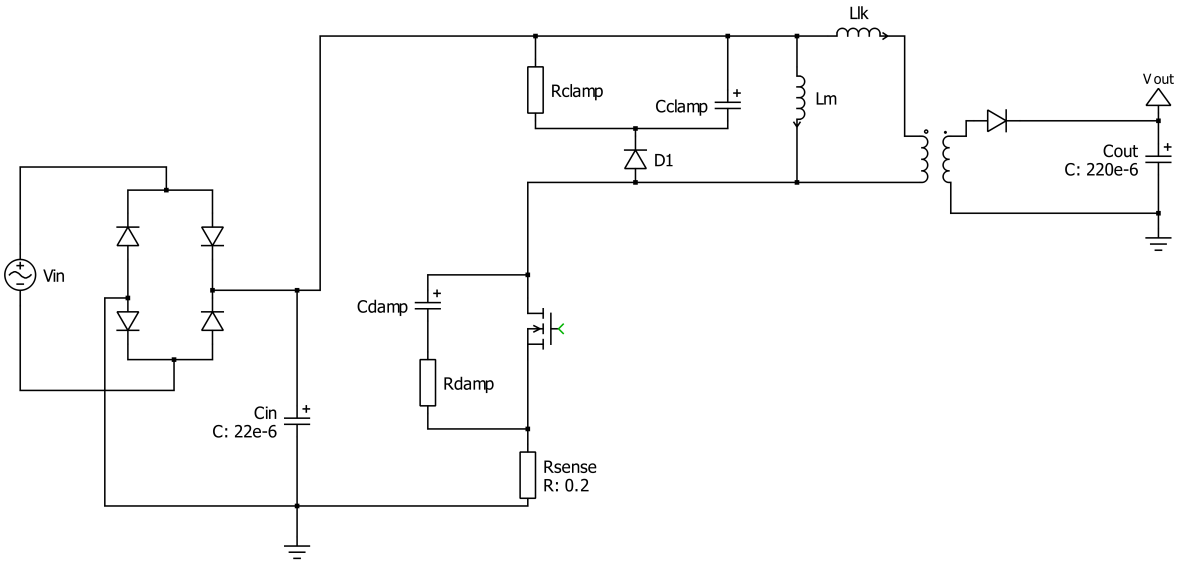

Figure 15 – Open loop designed Flyback converter.

3.3.1 Control System Design

In order to design a stable feedback control system, the phase margin test should be investigated and checked for any possible instability. However, the transfer function for each block in Figure 12 should first be established before the closed loop transfer function can be investigated.

Moreover, the control system for this project is designed to provide the CC-CV charging profile. In other words, the stability should be checked for both current and voltage control loops. Furthermore, both control systems were designed according to Section 2.3.

3.3.1.1 Voltage Control Feedback Design

The output voltage can be controlled using the process described in Section 2.3. However, it is necessary to study and a establish the transfer function for the Flyback power stage and then the feedback loop and compensator $G_c(s)$. According to (WANG, 2014), Equation (3.1) defines the transfer function of the Pulse-width modulator and converter power stage of Figure 12, or $\frac{1}{V_m}G_{vd}(s)$, for a Flyback converter in DCM operation.

$$G_v(s) = \frac{\hat{v}_o(s)}{\hat{v}_c(s)} = G_O \frac{(1+\frac{s}{w_{z1}})(1-\frac{s}{w_{z2}})}{(1+\frac{s}{w_{p1}})(1+\frac{s}{w_{p2}})} \tag{3.1}$$

where

$$G_o = V_{in}\frac{1}{V_m}\sqrt{\frac{f_s R_o}{2L_p}}\frac{1}{S_n+S_e} \tag{3.2}$$

$$w_{p1} = \frac{2}{R_{out}C_{out}} \tag{3.3}$$

$$w_{p2} = 2f_s\left(\frac{\frac{1}{D}}{(1+\frac{1}{M})}\right)^2 \tag{3.4}$$

$$w_{z1} = \frac{1}{R_{esr}C_{out}} \tag{3.5}$$

$$w_{z2} = \frac{n^2 R_{out}}{M(1+M)L_p} \tag{3.6}$$

For the equations above, S_n is the voltage slope when the primary-side current is detected on the current sense resistor, S_e is the slope of an externally added V_{ramp} (described in Section 2.3.1), which is not used in this project, making $S_e = 0$. M is the voltage transfer ratio nV_o/V_{in} and $n = N_p/N_s$. The PWM controller used in this project is based on the UCC38C4x current mode controller series from *Texas Instruments*, and V_m is acquired by a resistive divider inside the integrated circuit, being equivalent to 3 (INSTRUMENTS, 2022). Also, D is the expected steady state duty cycle, given by Equation (2.14). Finally, R_{esr} is the equivalent series resistor of the output capacitance.

Thus, in small-signal model of DCM, the power circuit has two poles and two zeros. Also, from the transfer function and the equations above, some poles and zeros are fixed such as the zero from the output capacitance and the equivalent series resistance ESR. Nevertheless, most poles and zeros a influenced by the operating point, which describes the operating condition of the circuit and is specified by the input voltage and the load current condition.

Therefore, the control system for this project considers the nominal input voltage of 220 V_{rms} and the maximum load of 21 $V/1.625\ A = 12.92\ \Omega$ which when added to the other parameters previously described provides the power stage with the Bode diagram in Figure 16.

It can be observed that the phase margin for the open loop converter is approximately $\phi_m = 145°$ at a crossover frequency of $f_c = 9\ kHz$, indicating stability. However, it can also be noted, from the magnitude frequency response, that high frequency components are not effectively attenuated. So when designing the closed loop system, it is necessary to reevaluate the phase margin, in case the new complete transfer function might have right half-plane poles, and also have the high frequency components attenuated (ERICKSON; MAKSIMOVIC, 2007; BASSO, 2012; MITCHELL; MAMMANO, 2001).

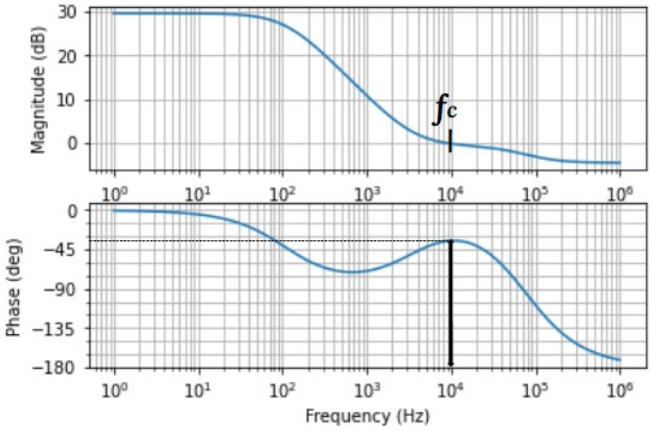

Figure 16 – Bode diagram of the Flyback power stage.

The feedback and the compensation network were constructed based on the system explored in Section 2.3.3.1. The optocoupler was designed based on the optocoupler PC817b, which has a CTR of around 1.75 (FIRST SILICON, 2016). Figure 17 shows the output voltage compensation network G_c designed for the project. The values for the voltage feedback system is presented in Table 5 and were chosen to provide stability. The stability was ensured by the phase margin test through the Bode diagram for $G(s) = G_c(s)G_v(s)$ shown in Figure 18.

The Bode diagram in Figure 18 shows that the phase margin for the output voltage feeback network is $\phi_m = 75°$ at the crossover frequency of $f_c = 5\ kHz$. Therefore, the phase margin is positive $G(s)/(1 + G(s))$ does not contain right half-plane poles, and the feedback system is stable.

Although the system was designed considering the operating point with the maximum output voltage, the system can be adapted for the lower desired output voltages of $V_{out} = 12.6\ V$ and $V_{out} = 16.8\ V$ by changing the value of R_1 to 4.04 $k\Omega$ and 5.72 $k\Omega$, respectively. The R_1 value is responsible to define the large signal value of V_{out} according

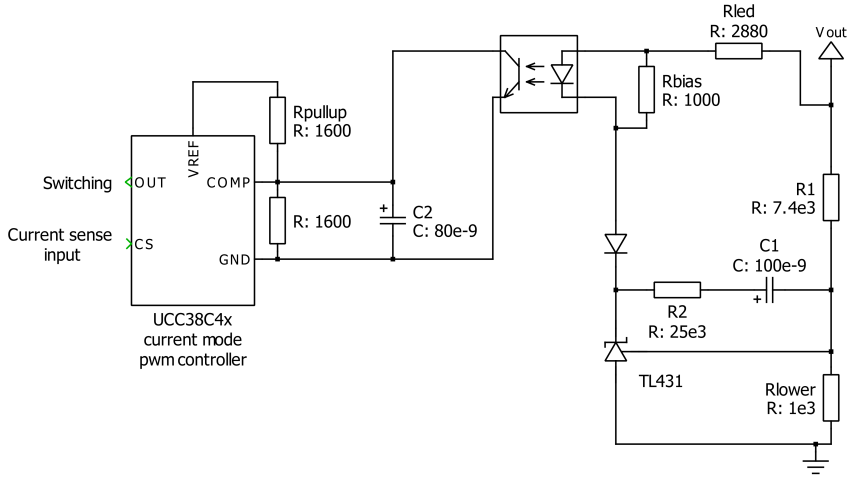

Figure 17 – TL431 based compensation network designed.

Table 5 – Output voltage compensation network parameters.

Element	Value
R_{lower}	1 $k\Omega$
R_1	7.4 $k\Omega$
C_1	100 nF
R_2	25 $k\Omega$
R_{led}	2.88 $k\Omega$
R_{bias}	1 $k\Omega$
C_2	80 nF
R_{pullup}	1.6 $k\Omega$

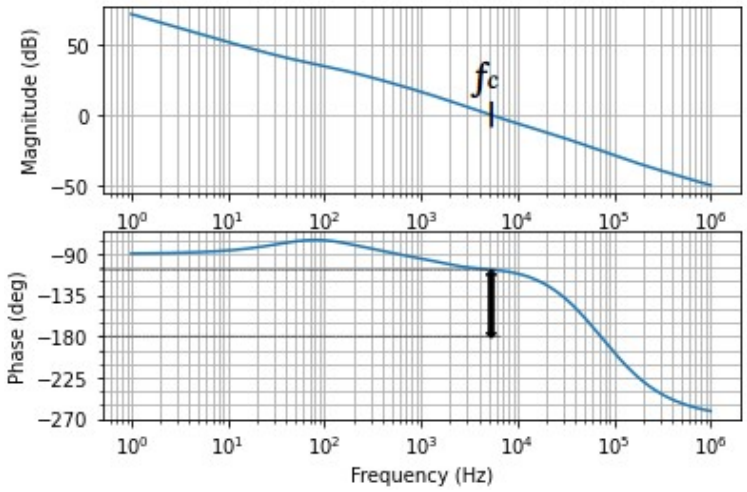

Figure 18 – Bode diagram of the loop gain $G(s)$ with voltage control.

to its combination as resistive divider with R_{lower}, as explained in Section 2.3.3.1. However, there is possibility for instability due to the feedback being constructed for another operating point, which will be checked and presented in the next chapter.

3.3.1.2 Current Control Feedback Design

Fundamentally, the current control system used in this project is a derivation of the voltage control implemented previously. Also, the goal is to limit the current, or control the current, when a load would demand more than the maximum power when operating at the nominal maximum output voltage. For example, when submitted to a load of 9 Ω, if there was only a output voltage feedback loop, the current would be of 2.33 A, which is above the target maximum output current of 1.625 A. However, if a stable current control feedback loop is applied, the error signal from it would be greater than that of the voltage loop and the current is controlled at 1.625 A, so the output voltage would be 14.625 V, instead of 21 V.

Therefore, in Figure 19 is presented the complete control system used. The current control feedback loop is also a TL431 based controller, explained in Chapter 2. It works by extracting the output current value through a shunt resistor, R_{shunt}, in series with the load. By using an operational amplifier, this R_{shunt} can be reduced, in order to reduce power dissipation, and its amplified sensed value is compared to the TL431 reference voltage. Thus, this combination can set the large signal value for the output current.

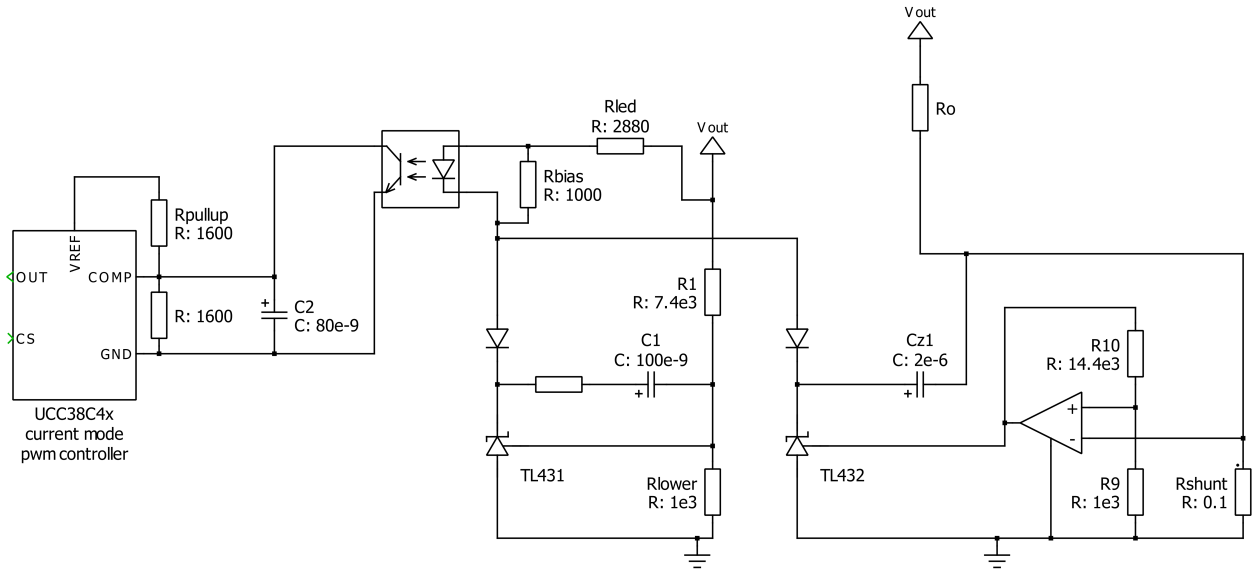

Figure 19 – TL431 based compensation network designed for voltage and current control.

Nonetheless, it is necessary to check for stability. Thus, in order to apply the phase margin test for this control loop, its transfer function needs to be established. Basically, the same method used in Section 2.3.3.1 is implemented for current control feedback loop. Although it is a method applied to control the output current, the output voltage is used build the transfer function through the Ohm's law. Equation (3.7) shows the controller's transfer function.

$$G_c(s) = -CTR\frac{R_{pullup}}{R_{LED}}\frac{1+1/sR_oC_{z1}}{1+sR_{pullup}C_2} = -G_0\frac{1+\omega_z/s}{1+s/\omega_p} \tag{3.7}$$

Where

$$G_0 = CTR\frac{R_{pullup}}{R_{LED}} \tag{3.8}$$

$$\omega_z = \frac{1}{R_oC_1} \tag{3.9}$$

$$\omega_p = \frac{1}{R_{pullup}C_2} \tag{3.10}$$

The operating point affects the zero in ω_z, since it depends on the load R_o. Consequently, this control system was designed for $R_o = 5\ \Omega$, which without a current control loop would result in an output current of $4.2\ A$.

The bode diagram in Figure 20 shows that the phase margin for the output current feedback network is $\phi_m = 80°$ at the crossover frequency of $f_c = 1.7\ kHz$. Therefore, the phase margin is positive and $G(s)/(1+G(s))$ do not contain right half-plane poles, and the feedback system is stable.

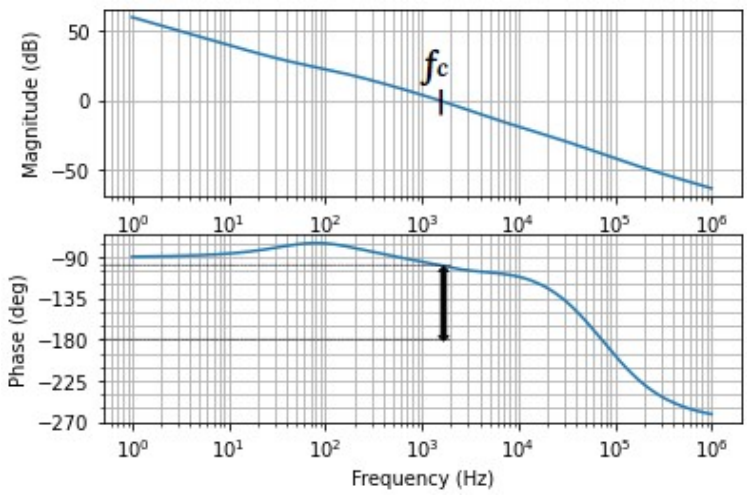

Figure 20 – Bode diagram of the loop gain $G(s)$ with current control.

Finally, the complete system is shown in Figure 21. In the next chapter, this circuit is analyzed when submitted to different load conditions and control configurations in order to check for capabilities to accurately and safely charge the battery targeted battery packs.

The Flyback converter and its control system designed was analyzed for different restive load conditions, in order to study the circuit response when submitted to situation similar to the battery packs desired to be recharge. Ideally, simulating with a battery would

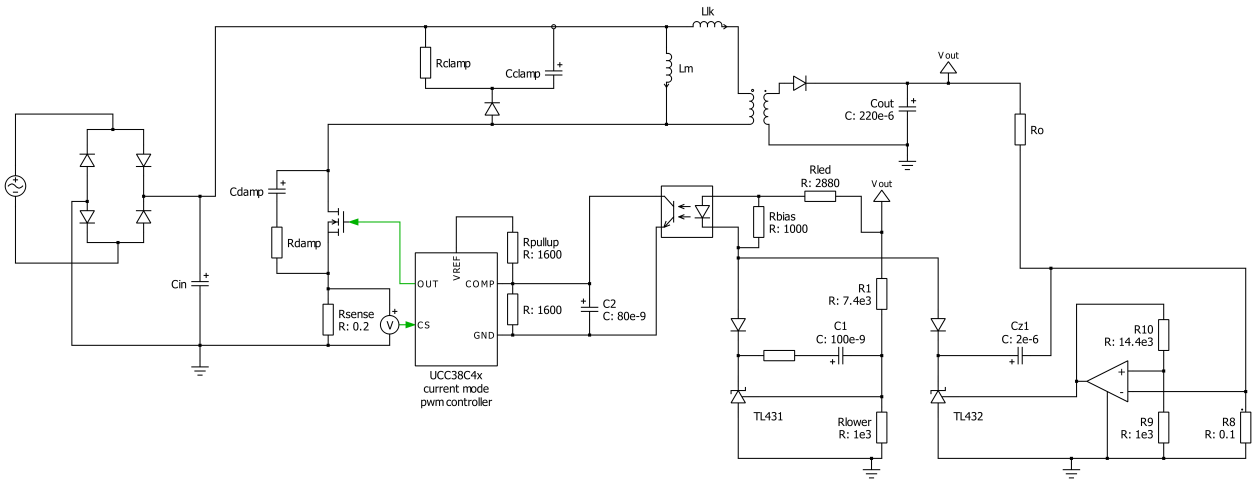

Figure 21 – Complete Flyback converter system designed.

give better and more precise data. However, due to the switching characteristics of the converter simulating with a precise battery model would imply a slow and computationally demanding simulation.

4 Results and Discussion

4.1 DCM Operation and Snubbers

The first aspects analyzed were the accurate DCM operation, and the clamping and damping snubber results. The conditions to which these parameters were analyzed were the nominal operation: $V_{in} = 220\ V$ and $R_o = 21\ V\ /\ 1.625\ A = 12.92\ \Omega$.

Figure 22 shows the MOSFET's drain voltage and the primary and secondary side inductor currents without the application of snubbers circuits. As a comparison, Figure 23 presents the MOSFET's drain voltage and the inductor's primary and secondary side currents with snubbers circuits applied. Not only the resonant effects were largely damped by the RC-Damping snubber, but also there was a great difference in the peak MOSFET's drain voltage, which was reduced from 1000 V to 546 V with the RCD-Clamping snubber.

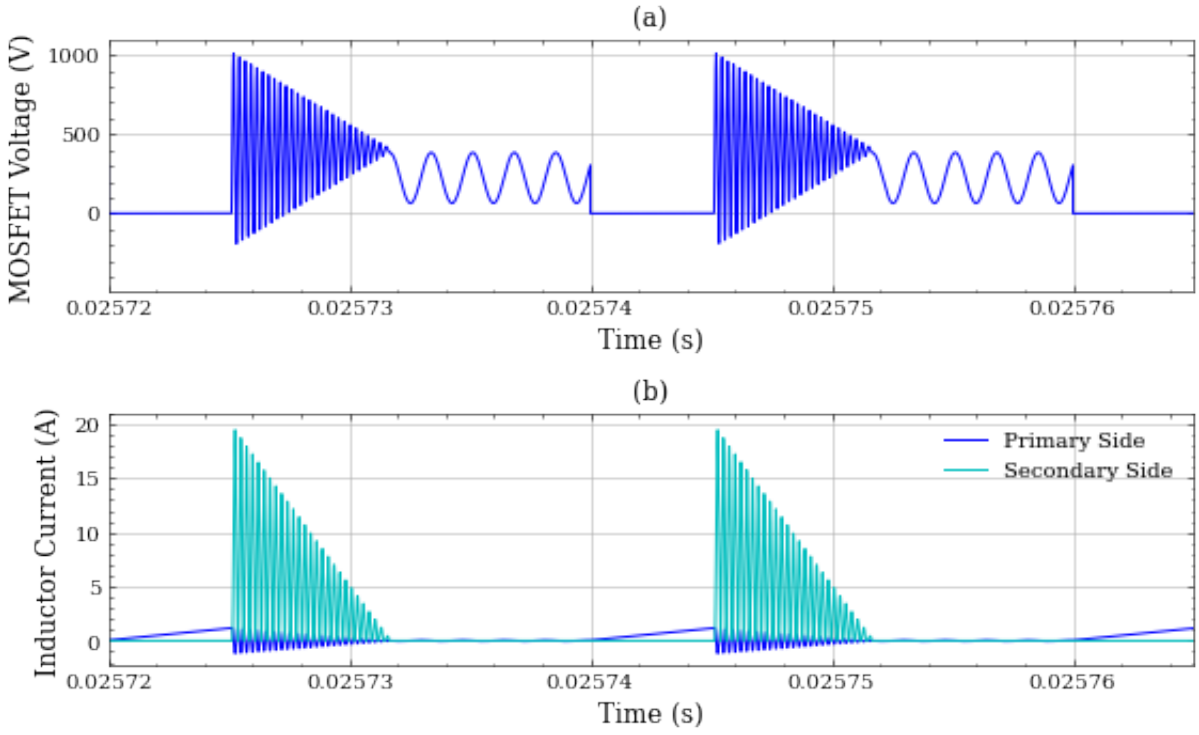

Figure 22 – MOSFET's drain voltage and the inductor primary and secondary side current at nominal conditions without snubbers.

From Figure 23, it is possible to observe that the design has DCM operation. When the switch is on, the current on the primary side of the the inductor increases linearly, and when the switch turns off the energy starts to deplete on the secondary, where the inductor current decreases linearly, until it reaches the dead time, where no

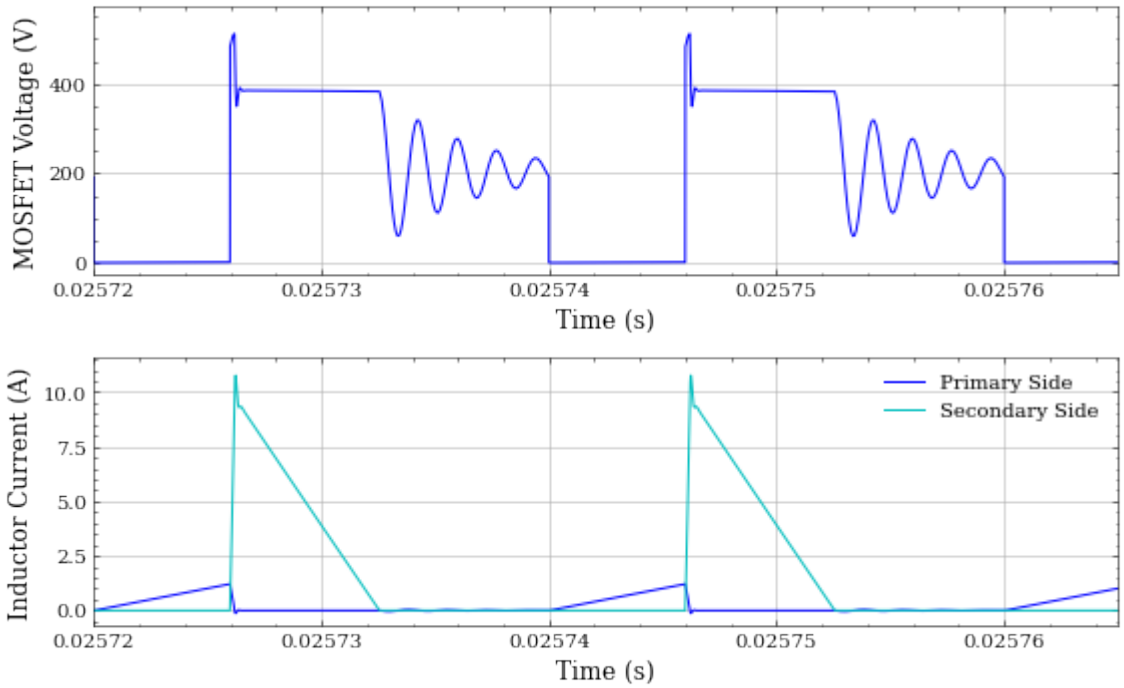

Figure 23 – MOSFET's drain voltage and the inductor primary and secondary side current at nominal conditions.

current flows through the transformer and ringing is observed on the MOSFET's drain voltage, caused by the magnetizing inductance and the MOSFET's C_{oss}, as explained in Chapter 2. The steady state duty cycle obtained was $D = 0.28$. Also, the peak current on each side of the inductor reflects the windings relationship of the transformer, $N = I_{speak}/I_{ppeak} = 11.07\ A\ /\ 1.24\ A = 8.93$, presenting a difference of 4.7 % compared to the set value of $N = 8.4$, due to leakage inductance and other non-ideal characteristics considered.

4.2 Voltage Control

The output voltage control was tested under two conditions and the value of R_1 was varied in order to change large signal voltage set value as explained in Chapter 3 and shown in Table 6. The voltage output value is modified so the system can be able to be applied to the different battery cells associations shown in Table 1, explained in the previous chapter. The first condition was implemented to check the voltage control under light load conditions ($R_o = 20\ \Omega$), then the circuit was submitted to the full load conditions.

For $R_o = 20\ \Omega$ the output set value was varied according to Table 6 and the output voltage response obtained for each case is shown in Figure 24.

Table 6 – R_1 and the expected V_{out} value.

R_1	V_{out}
7.4 $k\Omega$	21 V
5.72 $k\Omega$	16.8 V
4.04 $k\Omega$	12.6 V

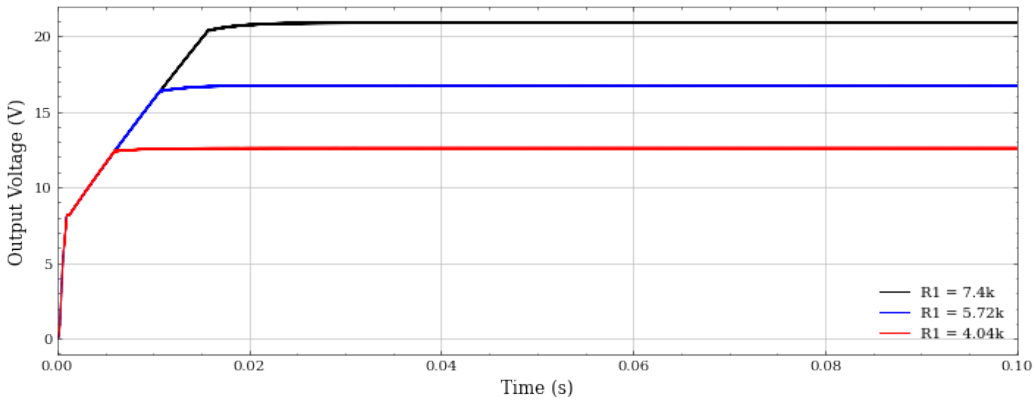

Figure 24 – V_{out} for each R_1 case under light load conditions.

Figure 24 shows that under light load the output voltage responses are stable and the steady state output average values found and their respective errors are shown in Table 7.

Table 7 – Steady state V_{out} value under light load conditions.

V_{out}	Average Error
20.85 V	0.71%
16.72 V	0.48%
12.57 V	0.23%

For the full load conditions, the load was varied accordance to the maximum power that can be delivered to each battery pack, in other words, the set voltage value and the maximum output current $I_{out} = 1.625A$. Figure 25 shows the voltage response obtained for each case. The steady state values obtained are shown in Table 8. For the cases of $R_1 = 7.4\ k\Omega$ and $R_1 = 5.72\ k\Omega$ the steady state average values were the same as before, with a output voltage ripple of 0.0028 V and 0.0025 V, respectively. However, when R_1 is set to 4.04 $k\Omega$, the average error for the steady state value increases and it shows a voltage output ripple of 0.94 V.

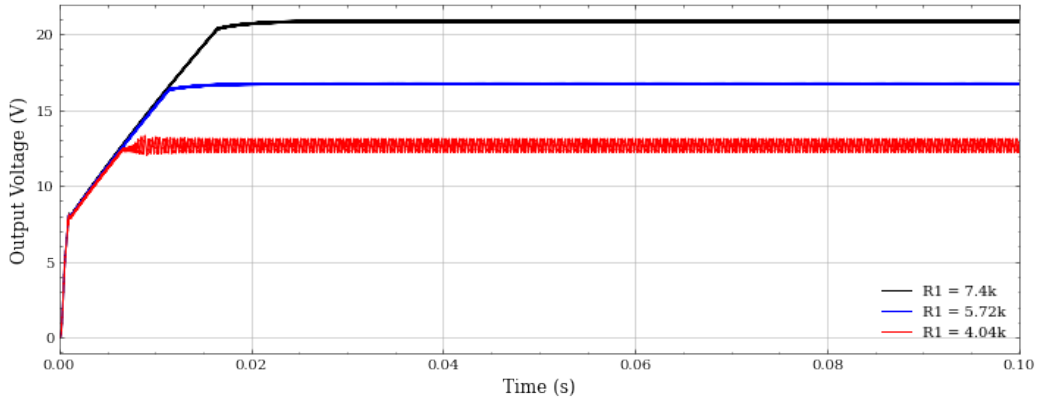

Figure 25 – V_{out} for each R_1 case under full load conditions.

Table 8 – Steady state V_{out} value under full load conditions.

V_{out}	Average Error
21.85 V	0.71%
16.72 V	0.48%
12.66 V	0.47%

4.3 Current Control

In order to verify the current control system designed, each condition of the circuit was submitted to a load that would be equivalent to the respective current X voltage relationship on a fully discharged battery pack (when all cells had a voltage of around 2.8 V and the current is 1.625 A). Figure 26 shows the output current response for each studied case. Also, Table 9 presents the steady state average value for each study and the errors obtained when compared to the target value of 1.625 A

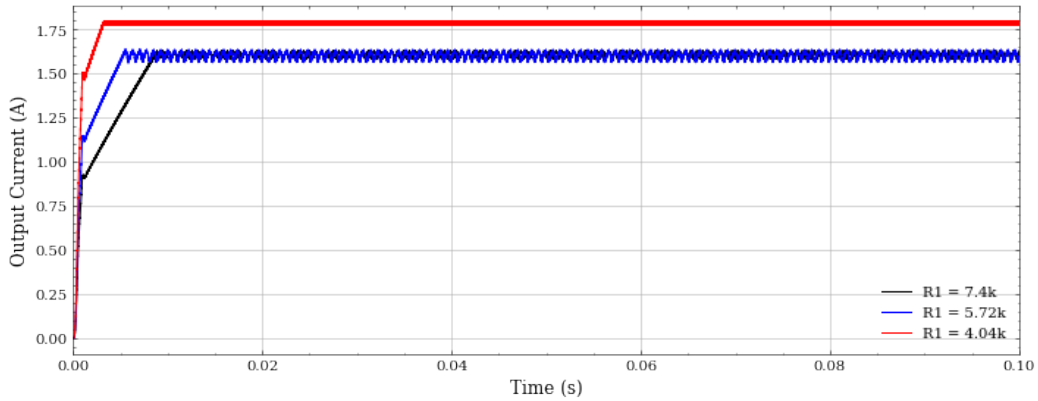

Figure 26 – I_{out} for each R_1 case under fully discharged battery pack conditions.

As observed, the values for the higher voltages with $R_1 = 7.4\ k\Omega$ and $R_1 = 5.72\ k\Omega$ have the current under the specified condition and could provide a safe amount of current

Table 9 – Steady state I_{out} under fully discharged battery pack conditions.

R_1	I_{out}	Average Error
7.4 $k\Omega$	1.61 A	0.92%
5.72 $k\Omega$	1.60 A	1.53%
4.04 $k\Omega$	1.78 A	9.54%

during the CC stage of the CC-CV charging profile, while for the case with $R_1 = 4.04\ k\Omega$ the obtained value exceeds the limit by 0.155 A. Also, the amount of ripple observed in each cases was 0.046 A, 0.077 A and 0.017 A, respectively.

4.4 *CC-CV* Charging Profile

In order to study and observe the constant-current constant voltage output behavior a variable resistance was applied to each output condition. This resistance would start with the load value for a fully discharged battery pack for each case and would increase linearly at a rate of 30 Ω/s for the whole simulated time.

Therefore, 6 waveforms were obtained, one case analyzing both the output voltage and current.

Firstly, for the situation with $R_1 = 7.4\ k\Omega$, aiming to provide 1.625 A during the CC stage and 21 V during the CV stage, the waveforms achieved are presented in Figure 27. The control system was able to control the current during CC, as expected from the previous analysis, under 1.625 A, with an average value of 1.61 A, and, during CV, the voltage under 21 V with an average value of 20.85 V.

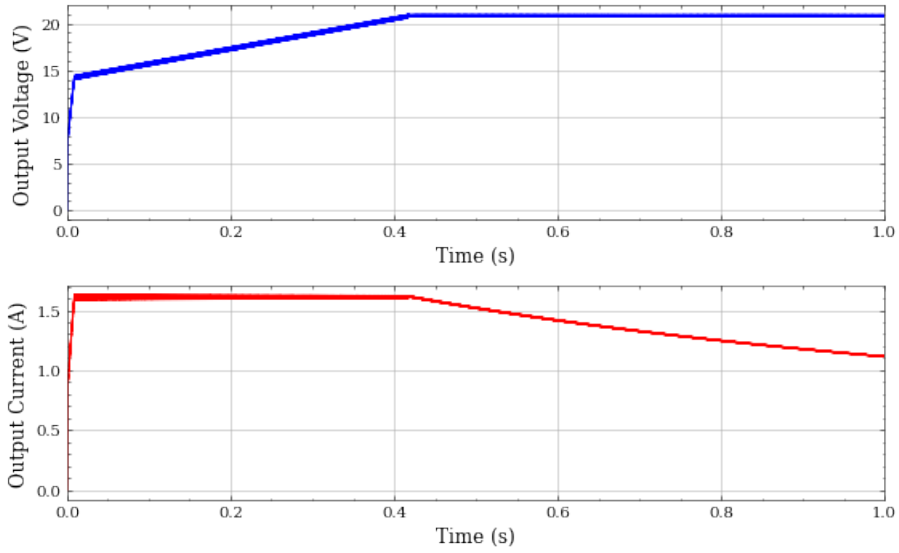

Figure 27 – *CC-CV* waveform: 1.625 A and 21 V.

For the case with $R_1 = 5.72.4\ k\Omega$, aiming to provide 1.625 A during the CC stage and 16.8 V during the CV stage, the waveforms achieved are presented in Figure 28. The control system presented a controlled current during CC under 1.625 A with an average value of 1.60 A, and, during CV, the voltage under 16.8 V with an average value of 16.72 V.

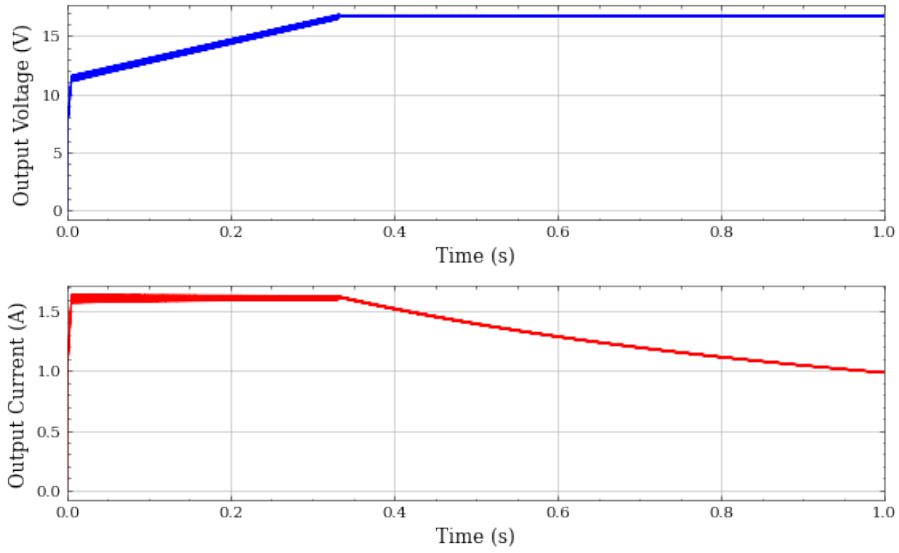

Figure 28 – *CC-CV* waveform: 1.625 A and 16.8 V.

Lastly, when aiming to provide 1.625 A during the CC stage and 12.6 V during the CV, the outputs observed are shown in Figure 29.

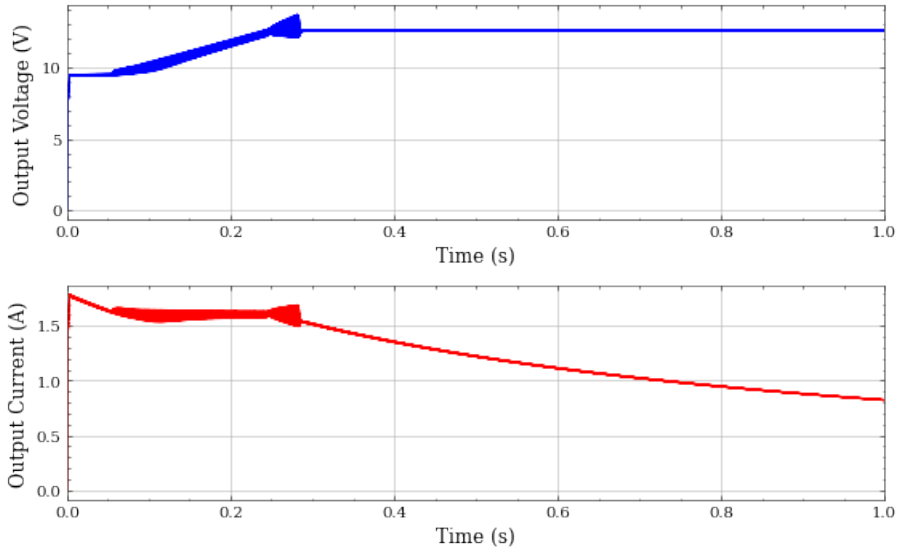

Figure 29 – *CC-CV* waveform: 1.625 A and 12.6 V.

As expected from previous analysis, for the case of fully discharged battery load, the current surpasses the aimed value, and when the maximum load is reached the output voltage has a greater output ripple, repeating the behavior observed when the voltage

control was studied under full load conditions in Figure 25, but now the ripple reached 1.298 V, reaching almost 13.968 V. However, when the load starts to decrease the output voltage is controlled and is under the 12.6 V value, with 12.57 V.

5 Conclusions

This work aimed to describe, analyze and model a DCM Flyback converter. Also, by using the secondary side feedback approach for an isolated DC-DC converter, it was demonstrated how the voltage control system can be designed and its output voltage can be varied. Furthermore, the traditional voltage control feedback was adapted to implement the current control system to provide CC-CV fast charging method used to recharge batteries.

Therefore, the system was modeled to be able to recharge the NCR18650B based in different series configurations using the variable output voltage and the current control method providing CC-CV charging. The peak current control PWM was used and the control system was checked for stability using the phase margin test.

The converter was then implemented using the software *PLECS* and after DCM operation was analyzed through the inductor and MOSFET waveforms. The resonant effects of DCM Flyback converters were analyzed and mitigated by the use of snubbers. The output was submitted to different load parameters in order to validate the control system. The system was stable and showed that for cases with 4 and 5 in series battery cells it could provide operation within the specified parameters. In other words the voltage could be controlled for the CV phase and the current for the CC phase within the battery cells specified parameters. However, when operating for 3 in series battery cells it showed that for high load conditions the output voltage showed a ripple that could damage the battery and current higher than the specified.

5.1 Final Considerations

It is very challenging to build a control system to operate in a broad range of variable output voltage. Mainly, it is designed for one specific condition and it can be implemented to a margin of that condition. As was seen is this work, varying from 21 V to 16.8 V could provide the desired operation, but for the 12.6 V case the results were slightly different than the expectations when full load condition was applied.

Nevertheless, the system could be redesign to avoid full load conditions for the 12.6 V case, by changing the current control setting the a value lower than 1.625 A, which would imply a longer charging time but could avoid damaging the batteries.

5.2 Continuity Proposals

For future developments of this research, the following studies may be suggested:

1. Simulate and analyze the system with a battery model with *PLECS* software.
2. Change the voltage range or the current setting so it can provide safe CC-CV charging for the battery pack with 3 battery cells in series.
3. Create and develop a hardware prototype to check and study the results on a prototype level.
4. Study how to implement a battery management system to the batteries to provide better and safer charging.
5. Increase the voltage range by using the AC stacking method.

Bibliography

ALATAI, S. et al. A review on state-of-the-art power converters: Bidirectional, resonant, multilevel converters and their derivatives. *Applied Sciences*, MDPI, v. 11, n. 21, p. 10172, 2021. Citado na página 19.

BASSO, C. P. Designing control loops for linear and switching power supplies: a tutorial guide. Artech house, 2012. Citado 6 vezes nas páginas 8, 35, 36, 37, 38, and 43.

BASSO, C. P. *Switch-mode power supplies*. [S.l.]: McGraw-Hill Education, 2014. Citado 4 vezes nas páginas 8, 27, 34, and 35.

BETTEN, J. Power tips# 98: Designing a dcm flyback converter. *EDN, May*, 2020. Citado 4 vezes nas páginas 24, 25, 26, and 27.

CHEN, M.; RINCÓN-MORA, G. A. Accurate, compact, and power-efficient li-ion battery charger circuit. *IEEE Transactions on Circuits and Systems II: Express Briefs*, IEEE, v. 53, n. 11, p. 1180–1184, 2006. Citado na página 17.

CHEN, S.-Y. Small-signal model for a flyback converter with peak current mode control. *IET Power Electronics*, Wiley Online Library, v. 7, n. 4, p. 805–810, 2014. Citado na página 32.

ERICKSON, R. W.; MAKSIMOVIC, D. *Fundamentals of power electronics*. [S.l.]: Springer Science & Business Media, 2007. Citado 9 vezes nas páginas 8, 23, 31, 32, 33, 34, 35, 38, and 43.

ESHKEVARI, A. L.; ZARE, M. Quasi-resonant switch-mode isolated lithium-ion battery charger with cc-cv modes of operations using secondary side controller. In: IEEE. *2017 Iranian Conference on Electrical Engineering (ICEE)*. [S.l.], 2017. p. 1101–1106. Citado na página 20.

ESHKEVARI, A. L.; ZARE, M. Quasi-resonant switch-mode isolated lithium-ion battery charger with cc-cv modes of operations using secondary side controller. In: IEEE. *2017 Iranian Conference on Electrical Engineering (ICEE)*. [S.l.], 2017. p. 1101–1106. Citado na página 21.

FIRST SILICON. *CHANNEL TRANSISTOR OUTPUT TYPE PHOTO COUPLER*. [S.l.], 2016. Rev. 0. Citado na página 43.

HART, D. W.; HART, D. W. *Power electronics*. [S.l.]: McGraw-Hill New York, 2011. v. 166. Citado na página 40.

HOQUE, M.; HANNAN, M.; MOHAMED, A. Optimal cc-cv charging of lithium-ion battery for charge equalization controller. In: IEEE. *2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES)*. [S.l.], 2016. p. 610–615. Citado na página 20.

INSTRUMENTS, T. Uccx8c4x bicmos low-power current-mode pwm controller. *Texas Instruments Incorporated, dostupno na URL: https://www.ti.com/document-viewer/ucc38c42/datasheet. pdf,[11. 2022.]*, 2022. Citado na página 42.

JHA, A.; SINGH, B. Portable battery charger for electric vehicles. In: IEEE. *2021 International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*. [S.l.], 2021. p. 1–6. Citado na página 21.

KLEEBCHAMPEE, W.; BUNLAKSANANUSORN, C. Modeling and control design of a current-mode controlled flyback converter with optocoupler feedback. In: IEEE. *2005 International Conference on Power Electronics and Drives Systems*. [S.l.], 2005. v. 1, p. 787–792. Citado 2 vezes nas páginas 8 and 33.

KUSHWAHA, R.; SINGH, B. An improved battery charger for electric vehicle with high power factor. In: IEEE. *2018 IEEE Industry Applications Society Annual Meeting (IAS)*. [S.l.], 2018. p. 1–8. Citado na página 20.

LIU, D. et al. Improved control strategy for t-type isolated dc/dc converters. *Journal of Power Electronics*, The Korean Institute of Power Electronics, v. 17, n. 4, p. 874–883, 2017. Citado na página 19.

MITCHELL, D.; MAMMANO, B. Designing stable control loops. In: *Texas Instruments Power Supply Design Seminar Notes*. [S.l.: s.n.], 2001. Citado 4 vezes nas páginas 31, 33, 35, and 43.

OUREMCHI, M. et al. Li-ion battery charger based on ldo regulator for portable device power management. In: IEEE. *2018 6th International Renewable and Sustainable Energy Conference (IRSEC)*. [S.l.], 2018. p. 1–4. Citado na página 17.

RAGHAVENDRA, K. V. G. et al. A comprehensive review of dc–dc converter topologies and modulation strategies with recent advances in solar photovoltaic systems. *Electronics*, MDPI, v. 9, n. 1, p. 31, 2019. Citado na página 19.

RIDLEY, R. Flyback converter snubber design. *Switching Power Magazine*, v. 12, 2005. Citado 2 vezes nas páginas 28 and 31.

SANYO ENERGY (U.S.A.) CORPORATION. *Lithium Ion Battery*. [S.l.], 2012. Rev. 1. Citado na página 39.

SCHLESINGER, R.; BIELA, J. Comparison of analytical transformer leakage inductance models: Accuracy vs. computational effort. In: IEEE. *2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*. [S.l.], 2019. p. P–1. Citado 2 vezes nas páginas 28 and 40.

SCHÖNBERGER, J. Design of a tl431-based controller for a flyback converter. *Plexim GmbH*, 2013. Citado 2 vezes nas páginas 36 and 38.

SEMINAR, P. S. D. Under the hood of flyback smps designs. *Texas Instruments Incorporated*, v. 2011, 2010. Citado 7 vezes nas páginas 8, 20, 23, 24, 25, 26, and 28.

SEMINAR, P. S. D. Common mistakes in flyback power supplies and how to fix them. *Texas Instruments Incorporated*, 2020. Citado 2 vezes nas páginas 19 and 24.

SINGH, B.; CHATURVEDI, G. D. Analysis, design and development of a single switch flyback buck-boost ac-dc converter for low power battery charging applications. *Journal of power electronics*, The Korean Institute of Power Electronics, v. 7, n. 4, p. 318–327, 2007. Citado na página 20.

SONST, M. *Verification Methods Of Snubber Circuits in Flyback Converters*. [S.l.], 2021. Citado 5 vezes nas páginas 8, 27, 28, 29, and 30.

SOUSA, G. J. de et al. A low cost flyback-based high power factor battery charger for ups applications. In: IEEE. *2009 Brazilian Power Electronics Conference*. [S.l.], 2009. p. 783–790. Citado na página 20.

SPORCK, C. *Battery Charger Fundamentals*. [S.l.], 2022. Citado na página 17.

TAR, B.; FAYED, A. An overview of the fundamentals of battery chargers. In: IEEE. *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*. [S.l.], 2016. p. 1–4. Citado 4 vezes nas páginas 8, 17, 18, and 19.

WANG, E. Feedback control design of off-line flyback converter. *Richtek Technology Corporation, Application Note AN017*, 2014. Citado 2 vezes nas páginas 32 and 42.

WOODING, G.; BEER, A. D. The effect of leakage inductance and snubbing on electromagnetic interference generated by a flyback converter. In: IEEE. *IEEE Africon'11*. [S.l.], 2011. p. 1–5. Citado 2 vezes nas páginas 28 and 40.