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DEPARTAMENTO DE ENGENHARIA ELÉTRICA

LUÍS OTÁVIO MACIEL DE OLIVEIRA

MODULAR MULTILEVEL CONVERTER: DESIGN, SIZING, CONTROL, SIMULATION AND APPLICATIONS

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Graduation thesis presented to the *Departamento de Engenharia Elétrica* from *Centro de Ciências Exatas e Tecnológicas* of the *Universidade Federal de Viçosa*, to obtain the credits from the course ELT 490 - Graduation Thesis and Seminar and fulfillment of a partial requirement for the degree of Bachelor of Electrical Engineering.
Advisor: Prof. Dr. José Carlos da Costa Campos.

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To my family, which "encouraged" me to enroll an University.
To my friends who invited me to drink and party.
To caffeine, which supported me during the nights of study and hard work.

Acknowledgment

I thank my family who supported me during every moment of my life, the teachers and mentors who have patience and trust in my work, all friends I acquired during the graduation which gave me the necessary support to complete this course. Thank CAPES for the opportunity to study in the Netherlands and CNPq for financial support in the researches I conducted, which helped developed this work.

"Start by doing what's necessary; then do what's possible; and suddenly you are doing the impossible."

Francis of Assisi

Abstract

The modular multilevel converter (MMC) has being increasingly used for medium/high-power applications due its advantages over the traditional converters topologies, especially the two and three-level voltage-source converter (VSC) for high-voltage direct current (HVDC) transmission system. Along with this the MMCs has being a subject of highlight within research groups.

Thus, this thesis is divided into two major parts. The first one provides a general overview of the MMC topologies along with submodules (SMs) circuit configurations, sizing of the MMC elements (SM capacitor and arm inductor), protection circuits and filters. The control techniques, simulation models with respective challenges are also carried out in the first part of this thesis along with a comparative study of the mathematical effort necessary to simulate the different models and the its accuracy.

The simulation of detailed MMC models requires a large computational time. Also engineer time is wasted in order to modify the number of submodules in these simulations. The second part of this graduation thesis develops a generic mathematical averaged-value model (AVM) based on state-space representation for a MMC. The results show that the use of the AVM represents with accuracy the MMC behavior with less processing time.

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1 Introduction

Nowadays, the converters used in power electronics are being constantly improved and needed for a wide range of applications. Furthermore, the demand for electricity has grown really fast in the last years (especially in economies such as China, India and Japan), bringing new challenges to these fields [1, 2]. As one of these applications, renewable power generation and transmission are one of the main areas where voltage-sourced converters (VSC) are required [3]. Currently, VSC are widely used for long-distances high voltage transmission, especially in the voltage-sourced converter based high voltage direct current (VSC-HVDC) [4, 5].

The increasing use of VSC-HVDC is mainly due to several advantages compared to line-commutated converter (LCC)-based HVDC transmission [6]. The construction of a VSC is based generally on insulated-gate bipolar transistors (IGBTs), controlled by pulse-width modulation (PWM) and it is able to control separately active and reactive power [7, 8]. A wide range of VSC-HVDC topologies have been used for different applications. The most used are: two-level, multilevel diode-clamped and floating capacitor multilevel converters [3].

Despite those traditional converters, a new trend has been observed with the use of modular multilevel converters (MMC), first proposed by Marquardt and Lesnicar in 2003 [9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20]. Comparing with other VSC topologies, in a MMC different voltage levels can be reached depending on: 1) the number of submodules (SMs), 2) the connection between the SMs, and 3) the SM topology. Higher number of SMs provides a better quality output voltage with very high efficiency, requires lower PWM switching frequency, reaches higher voltages and makes unnecessary the use of harmonic filters [20, 21]. However, increasing the number of submodules also requires a complex hardware to control the converter. The main advantages, control techniques and a complete overview about this topology are described in [22]. Gemmell *et al.* [9] summarizes the essential differences and advantages in the use of the MMC over familiar VSC topologies.

The high number of components in the MMC, especially IGBTs and capacitors, results in a challenge concerning modeling this converter in simulation software with detailed models (DMs). A small numerical integration time is important to reproduce accurately the converter behavior. Consequently, the necessary computing timing is increased. Furthermore, in order to modify the number of submodules or to change the submodule topology, it is necessary to modify the simulation model or even create a new one. Hence, simplified models or average-value models (AVMs) have been used in order to replicate with accuracy the converter operation with lower computing timing. The use of AVMs requires less computational processing and can use large incremental time [23]. Different approaches and reduced models have been studied and used for different analysis [19, 24, 25, 26, 27].

Although most of the AVMs produce good results, there are just a few models which include the submodules and the capacitors into account. These models are important in order to validate the control technique used, verifying the submodules capacitors voltage.

Over the last decade, the operation and control of different MMCs has been studied under many applications. The first part of this thesis provide a review about the uses of MMC. It will be focused on its topologies, sizing, protection circuits and filters. Chapter 2 introduces the MMCs topologies along with some SM circuit configurations that are used in the converter design. The components sizing, protection circuits and filters design will be present in Chapter 3. An overwien about the control techniques will be presented in

Chapter 4. Chapter 5 will discuss the different models used in order to simulate the converter while Chapter 6 will present the a performance study over each model described.

The second part of this thesis presents a generic mathematical model, based on state-space variables, to simulate a MMC with N submodules, it can be also implemented in any mathematical software including a method to reproduce both the system by state-space equations and the mathematical model. This study will be show in Chapter 7 along with a comparison between the DMs and the state-space model.

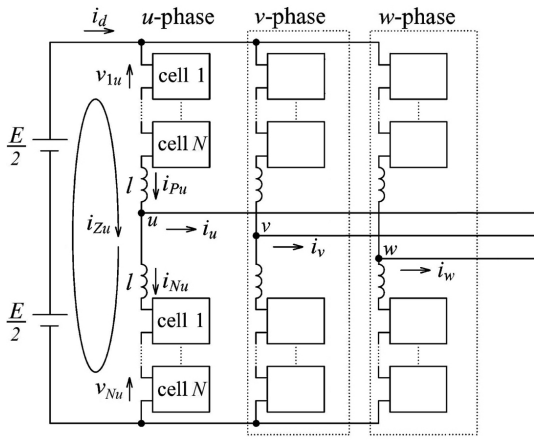
2 Converter Design

2.1 MMC Topology

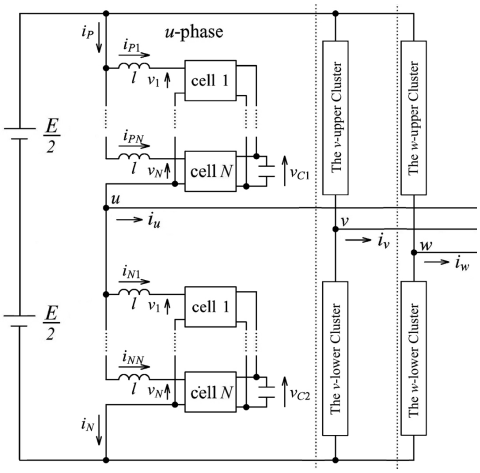
Figure 1 shows a design (schematic diagram) of four three-phase MMC topologies. The MMC consists in a connection between N SMs (normally in series connection) in order to produce the voltage levels required. The MMC also uses inductors (l) to suppress high-frequency components in the SMs current. These connections and components can be seen in Figure 1.

The MMCs topologies on Figure 1 can be divided as the following circuits:

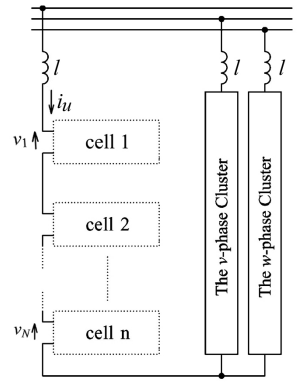
1. The double-star-configured (DSC) MMC [18, 28, 29, 30]: This topology requires a common dc-link (in our case represented by two voltage sources) with the purpose to charge the capacitors inside each SM and contribute to the output voltage, as show in Figure 1(a). The dc voltage, then number of submodules per arm N and the capacitors voltage will define the output voltage range that can be generated. An inductor l is connected in series with each set of SMs in each arm to suppress current



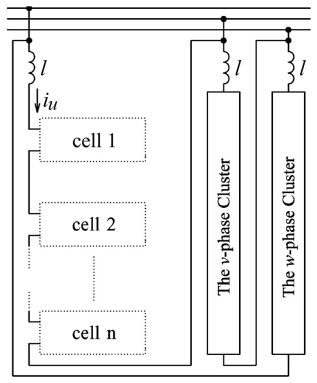
(a) The double-star-configured MMC.



(b) The dual MMC.



(c) The single-star-configured MMC.



(d) The single-delta-configured MMC.

Figure 1 – Circuit configuration of different MMCs.

ripples. In order to achieve better performance the two non coupled buffer inductors in each arm can be replaced by a single coupled inductor. The advantages of using a coupled inductor will be explained in Chapter 3. Based on its layout, the DSC can be used to generate as many output phases as required with different voltage levels and frequencies. The DSC topology is being used essentially in AC/DC converter and medium-voltage motor drives [31].

2. The dual MMC [28]: Although this topology is not well known its use becomes highly attractive for low-voltage large-current applications. Hagiwara *et al.* [28] proposed this topology based at the DSC topology. The differences between the dual MMC and the DSC are: the SMs connection, the common capacitor and the buffer inductors (l), as can be seen in Figure 1(b), . Each SM of the dual MMC has its own buffer inductor, and each compound set of inductor and SM is connected in parallel to each other and with a common dc capacitor. The dual MMC can be also used to generate different output phases. However, compared with the DSC, less current flows through the elements in this topology.

3. The single-star-configured (SSC) MMC [18, 30, 32]: The diagram configuration of this topology is shown in Figure 1(c). This topology uses a set of N SMs in series connection with a buffer inductor l for each phase. As can be seen, the MMC legs are connected in a star connection. Because of this layout, the SSC-MMC can be used only in three-phase systems. The SSC is mainly applied in static synchronous compensators (STATCOMs), SVC and battery energy storage system (BESS) [31].

4. The single-delta-configured (SDC) MMC [18, 30, 32]: The circuit configuration for this topology is shown Figure 1(d). The only difference between the SSC and the delta configured MMC: the delta connection between the arms, which affect the voltage and current ratings. The major uses for the SDC-MMC are the same as the SSC [31, 33].

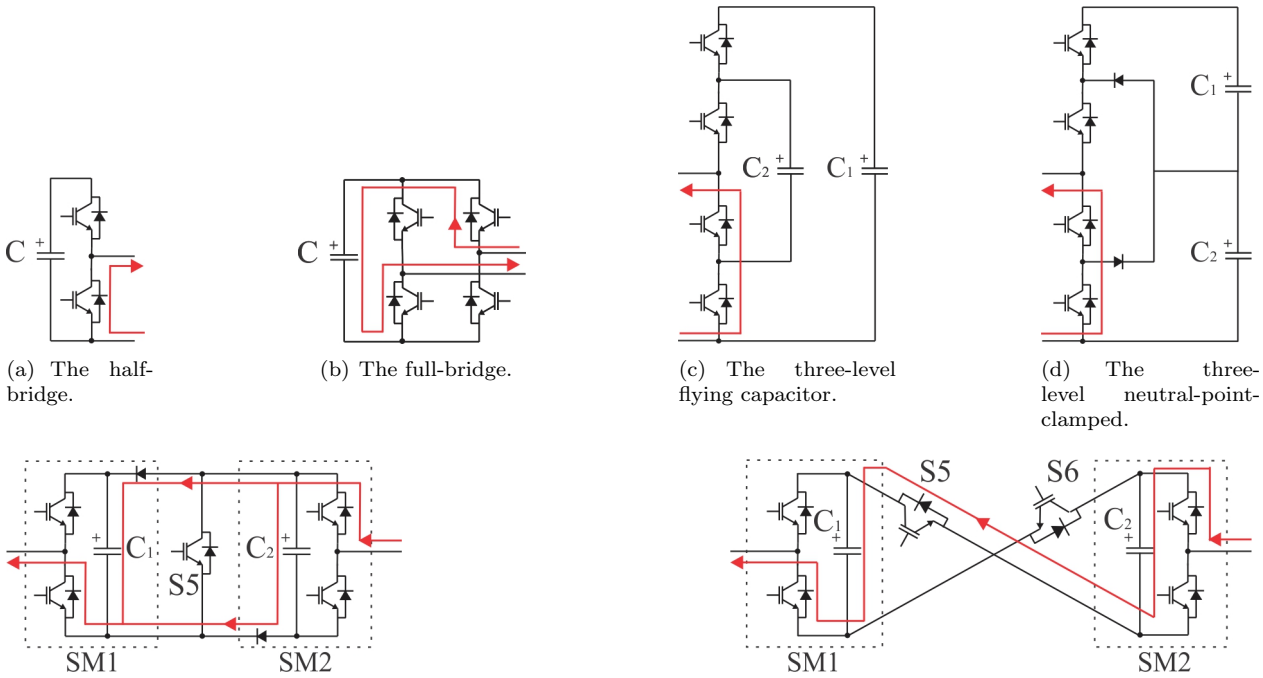
Different topologies from the ones listed in this thesis can be found for different applications. Among them the MMC in matrix configuration (consisting three star-configured in parallel) and hexagonal configuration (hexverter or 'double' delta configuration) are noteworthy [30, 31, 34]. They are used to interconnect different AC networks and in electric drive applications. These topologies have been proposed as alternatives to the typical AC/DC/AC back-to-back MMC configurations.

An interesting analysis has been made in [35, 36] with the use of a DSC-MMC based STATCOM with 4 legs to be connected in unbalanced systems. With the control of the fourth arm, responsible to handle the grid's zero-sequence current and voltage, the MMC is used for compensation of reactive power, harmonics and load balancing. With the same objectives an extended-MMC (EMMC) based on the SDC-MMC is proposed in [37]. Comparing with the MMC proposed in [35, 36, 37], the EMMC manage more accurately compensation for high-power applications.

Table 8 in Appendix A has summarized different characteristics of the most used topologies nowadays, using the same SM topology (full-bridge) [38]. However, the number of available topologies is constantly evolving and new topologies can be found for specific applications.

2.2 Submodules Topology

Plenty SMs topologies are design to achieve different voltage levels, power losses and in some cases offer a short-circuit fault handling capability for different applications. Figure 2 shows a schematic for the most used SM topologies [39] along with the current path under DC-fault operation. As can be seen, a SM consists



(a) The half-bridge.

(b) The full-bridge.

(c) The three-level flying capacitor.

(d) The three-level neutral-point-clamped.

(e) The clamp-double.

(f) The five-level cross-connected SM.

Figure 2 – Submodules configurations.

in a connection between capacitors, IGBTs and diodes. The IGBTs are responsible to insert the capacitors on the MMC arm, generating the desired voltage level.

The SMs topologies on Figure 2 can be described by the following circuits:

1. The half-bridge SM (HBSM) or chopper-cell circuit [2, 18, 28]: The HBSM is based on a cascade connection between two IGBTs and a capacitor, as shown in Figure 2(a). The output voltage of a HBSM is either the capacitor voltage v_c (when the SM is switched on) or zero (when the SM is switched off) depending on the switching states of the IGBTs [9, 11, 12].

2. The full-bridge SM (FBSM) circuit [2, 17, 18]: The FBSM can achieve 3 voltage levels depending on the switching states of the four IGBTs: zero, v_c and $-v_c$, as can be seen analyzing the possible IGBTs states in Figure 2(b),. Since the number of semiconductor devices in a FBSM are twice of HBSM, the switching losses and the cost of FBSM is higher than a HBSM. Although, this topology is able to limit the arms DC-fault currents. It can cut off arms currents by inserting the appropriate polarity of the capacitor in the arm [11].

3. The three-level SM (3LSM) circuit [40, 41]: The 3LSM is composed of both a three-level flying capacitor (3LSM-FC) and three-level neutral-point-clamped (3LSM-NPC), as shown in Figure 2(c) and 2(d). The switching losses are between the losses of a HBSM and the FBSM. However, the 3LSM does not provide a DC short-circuit proof feature such as the FBSM topology.

4. The clamp-double SM (CDSM) circuit [11]: The CDSM is composed of two HBSM interconnected by an IGBT $S5$ and two additional diodes, as shown in Figure 2(e). Under normal operation this IGBT is always switched on and the CDSM acts as a two series-connected HBSM. The CDSM has lower

semiconductor losses than the FBSM. As the full-bridge, this topology have the capability of blocking the dc-fault current.

5. The five-level cross-connected SM (5LCCSM) circuit [42]: The 5LCCSM consists of two HBSM interconnected back-to-back by two IGBTs, $S5$ and $S6$, as shown in Figure 2(f). This topology has the same semiconductor losses as the CDSM has and it can also block the short-circuit current.

Table 9 in Appendix A compares the SMs in terms of the semiconductor power losses and the required number of semiconductor components for the same MMC topology with 21 voltage levels [39].

Due to wide applicability of the MMCs, new MMC and SM topologies or hybrid designs have been made to achieve maximum performance with reliability. On the other hand, these topologies may not be commercially viable mainly due to patent protection.

Qin *et al.* [39] proposes a five hybrid MMC configurations (based on the combination of the HBSM and other SM topologies) with a dc-fault-handling capability (compared with the HBSM). They also have lower power losses and semiconductor device requirements than the required with the current topologies. Adam *et al.* [43] and Zeng *et al.* [44] present a hybrid MMC that combines FBSM and HBSM, which compared with the FBSM has the same dc-fault-handling capability using fewer semiconductor devices. Dargahi *et al.* [45] studies a modified topology for flying-capacitor multicell converters (FCMCs) as a modular submultilevel module capable to generate n voltage levels using n-1 cells. A series/parallel SM connection was proposed in [46]. The parallel SM connectivity reduces the conductivity losses and can be used for balancing the capacitors enabling stable operation of a MMC without monitoring the SM capacitor voltage.

3 Sizing and Design

All the elements which are in a MMC demands a correct sizing in order to behavior as we expect. This means, it must respect the grid codes requirements. The SM capacitance C for instance is sized in order to reduce voltage ripples or maximum energy ripple in the arms. However, the arm inductor l is chosen to suppress arm and circulating current. Although, the exact value of the arm inductance depends on the SM capacitor voltage, the modulation technique, the switching frequency and an additional controller optionally used for suppressing the circulating current. Along with that, a protection circuit should be inserted in the MMC in special cases (a circuit to bypass a SM when it is defective e.g.) and it may be necessary to use filters to improve the MMC operation.

Different topologies may require different sizing methods. This thesis will focus on the sizing of a DSC-MMC as shown in Figure 1(a) with HBSM. Nevertheless, each sizing technique is appropriated for an range of applications and the reader is encouraged to test different methods.

3.1 SM Capacitor

To control the energy ripple Kolb *et al.* [47] calculates the capacitance by

$$C = \frac{\Delta W_{max}}{N \cdot v_{C,avg} \cdot \Delta v_C} \tag{3.1}$$

where ΔW_{max} is the maximum energy pulsation (excess energy) in each arm, N is the number of SMs per arm, $v_{C,avg}$ is the average voltage value and Δv_C the voltage ripple of one SM calculated by

$$v_{C,avg} = \frac{v_{C,max} + v_{C,min}}{2} \tag{3.2}$$

$$\Delta v_C = \frac{1}{3}(v_{C,max} - v_{C,min}). \tag{3.3}$$

The minimum voltage $v_{C,min}$ is

$$v_{c,min} = E/N \tag{3.4}$$

where E is the DC-link voltage and the maximum voltage $v_{C,max}$ is sated by a portion of the nominal voltage of the capacitor used. The most adopted limit for this voltage is $1.1 v_{C,min}$.

Ilves *et al.* [48] proposes a capacitor sizing method for SMs with the capacitor reference voltage $v_{C,ref}$ different from the one described in (3.4) and the capacitor maximum voltage $v_{C,max}$ lower than the rated voltage of the SM, accordingly

$$v_{C,ref} = k_{dc} \cdot E/N \tag{3.5}$$

$$v_{C,max} \leq k_{max} \cdot E/N. \tag{3.6}$$

The minimum capacitance proposed is

$$C_{min} = \frac{2N \cdot \Delta W_{max}}{E^2({k_{max}}^2 - {k_{dc}}^2)}. \tag{3.7}$$

Figure 3 shows a graph with the capacitance value with different values of k_{max} and k_{dc} for a MMC with 5 SMs per arm, dc-link voltage $E = 600V$ and maximum energy pulsation $\Delta W_{max} = 30J$. This value was

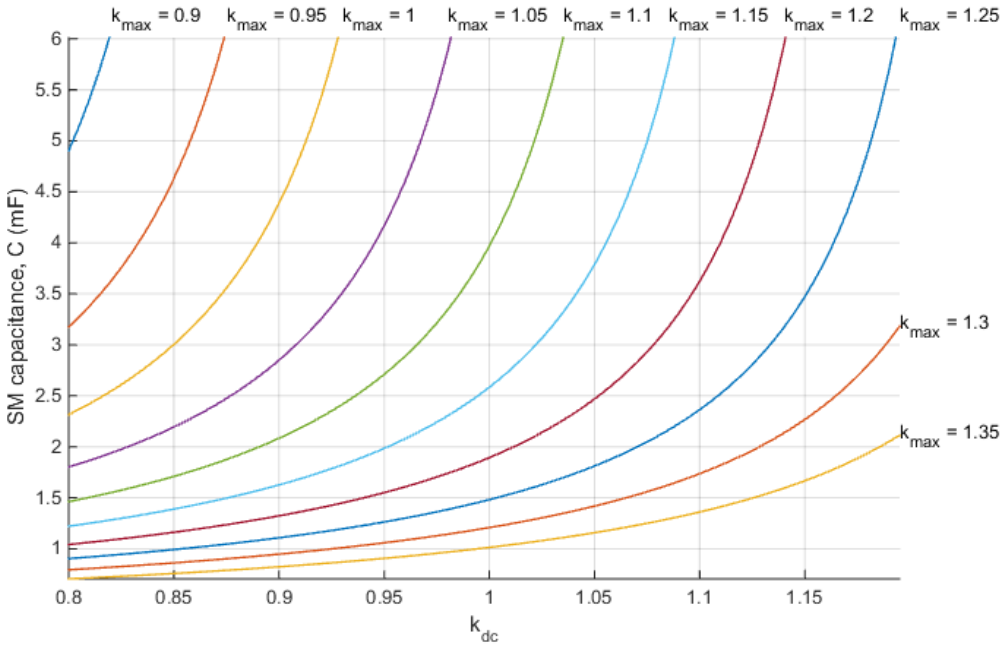


Figure 3 – Capacitance for different values of k_{max} and k_{dc}.

defined taking into account that in literature values between 20 and 40 KJ/MV are used for the energy W_{max} in each arm. Most applications uses $k_{dc} = 1$ and $k_{max} = 1.1$ but under special circumstances the MMC can operate with different values.

A capacitor sizing method based on the maximum energy stored in capacitors of a three-phase MMC E_{MMCmax} is proposed by Zygmanowski *et al.* [49]. The arm capacitance C_{arm} can be calculated using

$$C_{arm} = \frac{C}{N} = \frac{E_{MMCmax}}{3E^2} = \frac{2N \cdot E_{Cmax}}{E^2} \tag{3.8}$$

where E_{Cmax} is the maximum energy stored in one capacitor and it is assumed $v_{C,ref} = E/N$.

A capacitor size method which takes into account the load is used by Cunico *et al.* [50] and the minimum capacitance value is obtained by

$$C_{min} = \frac{2P_1}{v_c^2 \cdot \delta \cdot g_v \cdot \omega_o \cdot N} \sqrt{\left[1 - \left(\frac{g_v \cdot cos(\varphi)}{2}\right)^2\right]^3} \tag{3.9}$$

where P_1 is the single phase apparent power, ω_o is the fundamental frequency in radians, δ the percentage voltage ripple (%), $cos(\varphi)$ is the load power factor and with the voltage ratio

$$g_v = 2V_o/E \tag{3.10}$$

and V_o the peak value of the ac-side.

Figure 4 shows how the minimum capacitance C_{min} changes with different values of g_v and load displacement angle φ for a MMC with $P_1 = 150MW$, $\delta = 10$, $v_c = 120V$ and $\omega_o = 100\pi$.

3.2 Arm Inductor

Kolb *et al.* [47] proposes the arm inductor sizing to not exceed a maximum ripple circulating current $\Delta i_{Zx,max}$, in the phase x for DSC-MMCs which uses symmetrical triangular carrier signals to generate the

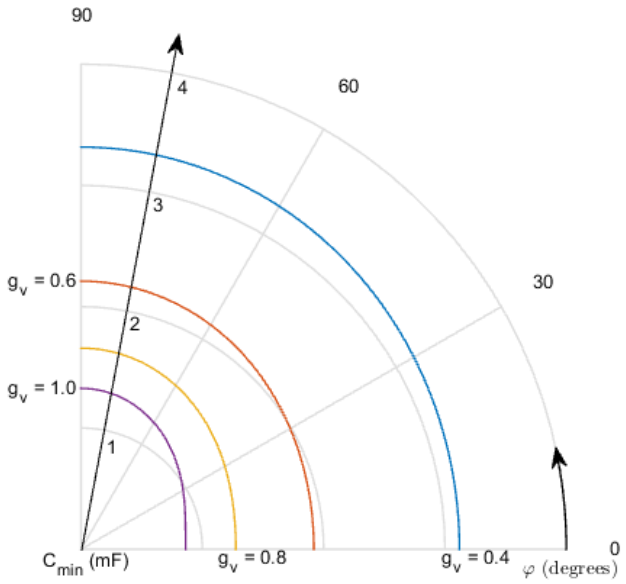


Figure 4 – C_{min} for different values of g_v and φ.

PWM signals. The circulating current i_{Zx} is calculated by

$$i_{Zx} = \frac{1}{2}(i_{Px} + i_{Nx}) \tag{3.11}$$

where i_{Px} and i_{Nx} are the upper and lower arm current respectively. The inductance can be obtained by

$$L = \frac{a_{Lx} \cdot T_a}{2\Delta i_{Zx}} \cdot \frac{v_{x,max}}{N} \tag{3.12}$$

where a_{Lx} is the duty cycle which causes the highest flux linkage (which depends on the modulation technique), T_a is the switching cycle and $v_{x,max}$ is the maximum SM voltage in a phase x (obtained by adding all SM maximum voltages).

Alternatively to this method in which is necessary to know the value of a_Lx, Tu *et al.* [51] uses a method to limits the peak value of the double-fundamental-frequency circulating current I_{2f}. Thus, the arm inductor is calculated by

$$L = \frac{1}{8{\omega_o}^2 \cdot C \cdot v_C}\left(\frac{P_s}{I_{2f}} + E\right) \tag{3.13}$$

where P_s the apparent power defined as

$$P_s = E \cdot i_d / cos(\varphi) \tag{3.14}$$

where i_d is the dc-link current.

The second inductor sizing method used by Tu *et al.* [51] consists in limiting the current rise in fault conditions. Since the worst considered fault case is a short circuit applied in the dc-link bus, the sum of the voltage of the SMs inserted during the fault is equal to E. Then,

$$l\frac{di_{Px}}{dt} + l\frac{di_{Nx}}{dt} - E = 0. \tag{3.15}$$

Since the upper and lower current are supposed to be equal during the fault $i_{Px} = i_{Nx}$, leading to:

$$\alpha = \frac{di_{Px}}{dt} = \frac{di_{Nx}}{dt} = \frac{E}{2l}. \tag{3.16}$$

And the inductor l is

$$l = \frac{E}{2\alpha}. \tag{3.17}$$

The inductor analysis proposed by Zygmanowski *et al.* [49] is based on the resonant effect that occur in both converter arms. The inductance is selected with the objective to suppress any high frequency components of arm currents. This can be done avoiding resonances in the circulating current for an arm capacitance C_{arm}, thus

$$l_r = \frac{1}{C_{arm} \cdot {\omega_o}^2} \frac{2(h^2-1) + m_a^2 \cdot h^2}{8h^2(h^2-1)}, \quad \text{for } h = 2n, n = 1, 2, \ldots, \infty \tag{3.18}$$

where l_r is the resonance arm inductance, h is the harmonic order and m_a the modulation index in which the MMC operates.

With the objective of suppress arm currents of second and fourth order in most applications a region with potentially high current harmonic can be found using (3.18). This region is composed by the area between inductance values for $h = 2$, $m_a = 1$ and $h = 4$, $m_a = 0.1$ which is indicated in Figure 5 for a fundamental frequency of 50 and 60 Hz. The arm inductance l should be outside this region, usually higher. Nevertheless, an arm inductance inside the warming region can be used if there is a circulating current suppression control [49].

3.3 Alternative Methods

Pirouz *et al.* [35] determines the capacitance of the 4 legs MMC with HBSM discussed in Section II. The method takes into account the instantaneous current passing through each SM when its have the highest fluctuation of load current and the maximum voltage ripple Δv_C desired. The inductance is calculated using the capacitor reference voltage $v_{C,ref}$ given by (3.4), the switching frequency and the maximum arm current ripple desired. Alternatively, the capacitance can be calculated on the basis of the maximum dc-link voltage ripple, the switching frequency and the nominal current rating for each SM [36, 37].

A capacitor sizing based on the analysis on dc, first- and second-harmonic average arm current is proposed by Sztykiel *et al.* [52]. Based also in the 1st and 2nd harmonic arm currents, a criterion for sizing the arm

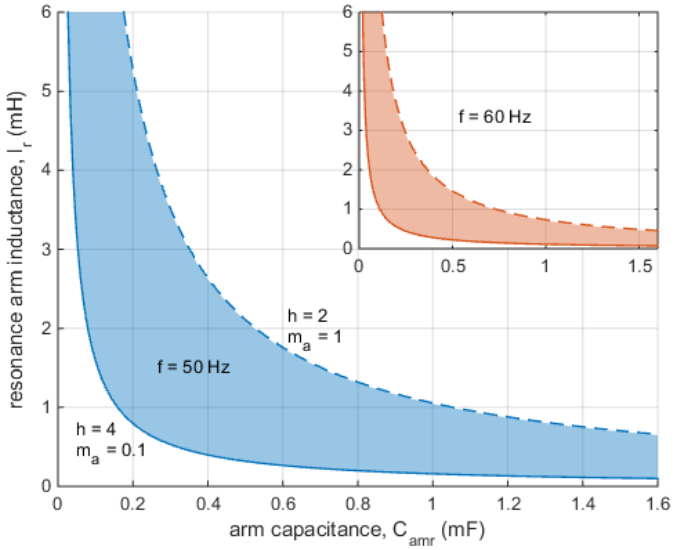


Figure 5 – Resonant inductance for different values of arm capacitance and fundamental frequency of 50 and 60 Hz.

inductor is used along with the maximum rate of change of a possible dc short-circuit between arms. The chosen inductance is the higher one obtained from the two sizing methods. Merlin *et al.* [53] uses a method based on the same principle as the one used in (3.1) for different MMC topologies comparing them. Hillers and Biela [54] presents a sizing method to MMCs for BESS which is based in (3.7) for the SM capacitor. The inductor used is based in a LCL-type filter using one inductor per arm and/or one for each phase. A sizing method is proposed taking into account the maximum current in case of fault, the grid voltage and the total delay in the control loop used.

A new trend has been observed with the use of a single coupled inductor instead the two noncoupled buffer inductor in each arm of a DSC-MMC. Compared with the noncouple inductor the single inductor presents reduction in size, weight and cost. Figure 6 shows the circuit configuration of a coupled inductor. In the DSC-MMC the terminals a and b are connected in the upper and lower arms respectively, while c is connected to the load.

Since the relation of $l_{ab} = 4l_{ac} = 4l_{bc}$ is presented in a coupled inductor, it does not affect i_o since the magnetic fluxes produced in i_P and i_N cancel each other [18, 28]. The use of couple inductor in a SDC-MMC can be found in [33]. Despite the advantages of using a coupled inductor, its use still not widespread.

Finally as recurrence, the parameters (C, C_{arm}, l, N, ...) chosen in different MMCs used in the literature are presented in [49].

3.4 Protection Circuit

Although the elements on a IGBT are sized for normal operation, when the MMC is submitted into special conditions a protection circuit needs to be inserted in order to not cause any damage to the MMC components.

The first condition to analyze is the start-up of an MMC. When the MMC starts all the capacitors are discharged and the current through an arm increases rapidly. To restrict the current peak value an easy solution is insert a circuit consisting in a resistor in parallel with a switch in series with either the dc-link, each phase (in a AC-DC converter) or each arm inductor. When the MMC starts the switch is turned off and the resistor is connected in the circuit until the capacitors charge-up, turning the switch on and removing the resistor [16, 18]. Into simulations, an arm resistance also needs to be inserted in series with the inductor representing inner inductor resistances and the converter losses. Analysis of MMCs in which the arm resistor (for start-up process or losses representation) are taken into consideration can be found in [18, 29, 30, 31, 48, 49].

Other situation which a protection circuit is demanded is when a short-circuit occurs. In the short circuit period the IGBTs are blocked but current continues to flow through anti-parallel diodes across the IGBTs. In a MMC using only SM topologies with no DC-fault-handling capability the current flows thought these diodes without the insertion of the SM capacitor in the circuit, as can be seen on Figure 2. Resulting in extremely high current and damage if the short circuit is not disconnected [11, 20]. Even though the arm

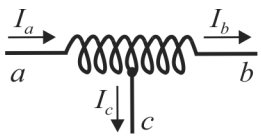


Figure 6 – Coupled inductor.

inductor has influence on the transient states, the final fault current is the arm and dc-link resistance, which are as low as possible [15]. Thus, DC breakers are being used for HVDC systems.

As example, Häfner *et al.* [55] proposes and tests a modular hybrid IGBT DC breaker for reliable dc grids in which the dc current needs to be interrupted within less than tens of ms with minimal losses. A schematic diagram for this DC breaker is shown in Figure 7, consisting in the main DC breaker (separated into several sections with individual arrester banks) in parallel with a fast mechanical disconnector and an auxiliary dc breaker. In a normal operation the current flows only through the bypass switch. When the dc fault occurs the auxiliary DC breaker commutates the current to the main DC breaker and the fast disconnector opens (with opening times below 2ms). Thus, with the mechanical switch in open position, the main DC breaker breaks the current. After fault clearance, the residual DC current breaker isolates the faulty line to protect the arrester banks of the hybrid DC breaker from thermal overload.

The SM fault also has to be considered. One of the most used and simple ways to remove the SM from the circuit is inserting a high-speed bypass switch between the SM terminals, represented by $K1$ in Figure 8. Then with adequate control, the SM is removed from the circuit and the terminal voltage becomes equal to zero. In some situations the capacitor voltage can also becomes zero. The use of bypass switches along with higher number of SM than the necessary, operating in conditions below their nominal values, are essential in MMCs for uninterpretable applications [9, 13, 14, 16, 41, 52].

In order to prevent high current through the elements in a SM a press-pack thyristor (known for their high capability to withstand surge currents) can be inserted in parallel with the SM terminals, represented by $T1$ in Figure 8. After detecting a high current throw the MMC arm (in a fault i.e.), the $T1$ is fired preserving the SM elements which have low capacity for withstanding surge current events related to their silicon surface, i.e. [13, 16, 41, 52].

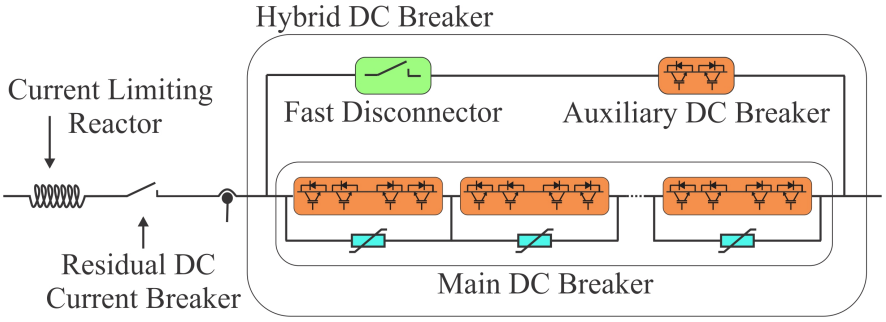


Figure 7 – Modular hybrid IGBT DC breaker.

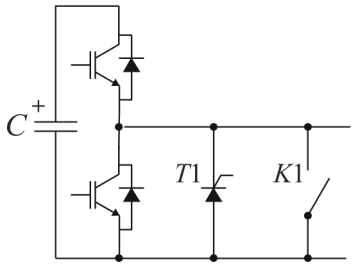


Figure 8 – Protective switches.

3.5 Filters

Higher numbers of SMs in a MMC implies in a better quality voltage output making the use of filters unnecessary [20]. Nevertheless, the quality of the voltage can be further improved using filter to eliminate the harmonics caused by the switching of the semiconductors i.e., and necessaries in weak grids or with MMC with small number of SM.

Sztykiel *et al.* [52] proposes the use of a high frequency filter for a AC-DC DSC-MMC. The filter is used for reactive power compensation at point of common coupling (between the arm inductors). The filter used is design as a 2nd order high-pass filter and modeled with a capacitor C_f in series with a set of an inductor L_f and a resistor R_f in parallel, as shown in Figure 9(a). The circuit is then connected between the point of common coupling and ground. The filter sizing is calculated from:

$$C_f = 6\left(\frac{I_{arm}}{V_{AC}}\right)^2 l \tag{3.19}$$

$$L_f = \frac{1}{C_f\sqrt{2\pi f_{res}}} \cong \frac{1}{C_f\sqrt{2\pi f_{sw}}} \tag{3.20}$$

$$R_f = 2\pi \cdot f_{res} \cdot L_f \cdot q \tag{3.21}$$

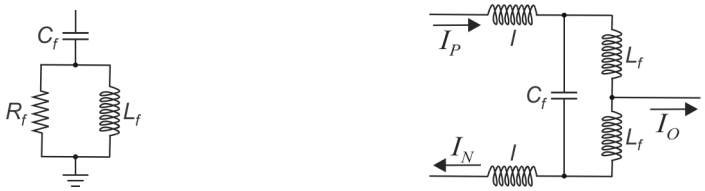
where I_{arm} is the arm current, V_{AC} is the equivalent AC voltage source (calculated using Thevenin), f_{res} is the resonant frequency, which should be close to effective switching frequency f_{sw} of the MMC converter and q is the quality factor [52].

Ilves *et al.* [56] proposes the use of a main-circuit filter, designed to block the 2nd order harmonic in the circulating current in a DC-AC DSC-MMC [57]. The main-filter is composed of two series inductor L_f in parallel with a capacitor C_f. The filter in then connected in series with the arm inductors, thus the ac side is now connected in the common coupling of the filter inductors as shown in Figure 9(b). The main filter capacitance is given by:

$$C_f = \frac{1}{8\omega_o^2 \cdot L_f} \tag{3.22}$$

from a arbitrary value of L_f [56].

As another example, Kolb *et al.* [58] implements a LC-filter in the ac-side of a DC-AC DSC-MMC with single coupled inductor. The filter used has also the objective of remove harmonics in the range of the switching frequency.



(a) High-pass filter.

(b) Main-filter.

Figure 9 – Filter used in a MMC.

4 Control Techniques

Despite the active, reactive (or positive and negative voltage sequence) and dc-bus voltage control using *abc*, $\alpha\beta$ or *dq* representation implemented in almost the totally of the converters [19, 24, 33, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72], the MMC requires some additional controllers in order to keep the system stable and achieve higher efficiency. The most common controls will be shown bellow.

4.1 Individual Balancing Control

All SMs capacitor voltages must be balanced and stable during normal operation [9]. Wherefore all the capacitor voltage needs to be controlled by changing the SM reference in order to insert or remove the capacitor from the circuit. To achieve this control techniques based on Balancing Control Algorithm (BCA) are been used.

The conventional BCA (also known as Reduced Switching-Frequency (RSF) voltage-balancing algorithm) [10, 12, 73, 74] requires the capacitor voltages and arm currents to be measured periodically, them the SMs are sorted in ascending order. Along with the number of SMs to be inserted given by the reference voltage desired and the PWM technique used the SMs to be turned on or off are selected as follow:

- If the arm current is in a direction to charge the capacitors, the SMs with lowest voltages are switched on while those with highest voltages are switched off.
- If the arm current is in a direction to discharge the capacitors, the SMs with highest voltages are switched on while those with lowest voltages are switched off.

The main drawback associate with this technique is the use of high switching frequency as the measurements are taken at every PWM period. A different BCA is found in [10, 75] where the SMs are switched ON or OFF only when the reference signals crosses one of the carrier waves on the Phase-Shift Pulse Width Modulation (PS-PWM) i.e. the number of SMs to be inserted changed. An modification in this method is proposed by Tu *et al.* [76] and can be summarized as follow:

- If an extra SM needs to be switched on, no switching is applied to those who are already inserted and the BCA will be used on those SMs in off-state.
- If an extra SM needs to be switched off, no switching is applied to those who are already bypassed and the BCA will be used on those SMs in on-state.

Compared to the conventional BCA method, these RSF voltage balancing algorithm reduces the device switching frequency and consequentially the total switching losses.

Although the BCAs described keep the average capacitor voltages constant yet may occurs a considerable voltage ripple on the capacitor as the switching frequency and number of SMs decrease. A BCA using proportional controller has been presented in [64] with the objective to forces each capacitor to follow the average voltage in its cluster (phase) of a SSC-MMC. Three BCAs similar controllers are presented in [28, 77] for a DSC-MMC and a HB-MMC using a constant reference instead the average. The first method multiples the output signal by the direction of the upper or lower arm currents (i.e. 1 if the current charges the capacitors and -1 otherwise), the second multiples it by the arm current value itself and the third method

multiples it by the MMC output current. The output signal is them added to the reference voltage signal of each SM.

Compared with the BCA methods described before these methods have the advantage of keeping the device switching frequency the same as the PWM carrier frequency and no need to sort the SMs based on the capacitor voltage. Nevertheless, the use of a proportional controller to each SM increases the mathematical effort on the controller used as the number of SM increase.

An BCA used in MMCs for a transformerless medium-voltage motor drive using the same principle as the third method described can be found in [78] using the arm voltage reference instead the arm current. The advantage is by using the voltage, the motor current is not affected during the start up process. A similar BCA as the first method is presented in [65] for a SSC-MMC. In this case the active power reference signal is used instead of the arm current signal to multiple the reference (i.e. 1 if the active reference power is positive and -1 otherwise).

4.2 Average Voltage Control

The voltage across each capacitor can controlled using BCA method. Although it depends on the arm current. An average voltage control can be used in order to give a reference for the circulating current control which will be explained in the next section. The controlled variable in this case is the average voltage over all capacitors.

A method Proportional Integral (PI) controller is presented in [28, 77]. The general idea is increase the circulating current value when the average voltage is bellow the set point and decrease its value otherwise. Then the capacitor voltages present a faster response and a stable value.

4.3 Cluster Balancing Control

Similar to the average voltage control this method has the objective to control not the average voltage across all capacitor but the average voltage across each MMC arm by given the reference for the arm currents, thus each arm requires a independently controller. Again this method is implemented by Hagiwara *et al.* using PI controllers for both DSC-MMC and HB-MMC [28, 77]. Its use in a SSC-MMC where the output of each cluster control is then added to give the reference for the circulating current control is demonstrated in [33].

Maharjan *et al.* [65] uses a series of proportional controllers to maintain the average voltage of each arm in a SSC-MMC equals to the dc mean voltage of all capacitors. The strategy is divided in a outer control responsible to give the dc arm current reference for the inner control, responsible to generate a reference to all capacitors in the cluster.

4.4 Circulating Current Control

This controller has the objective to control the circulating current or the MMC arm currents without affecting the output current. Hagiwara *et al.* implement a PI controller with the reference given by the average voltage in a SSC-MMC [28, 77] and a proportional controller with the reference from the cluster balancing control in a SSC-MMC [33]. The controller response is them added to the SM reference voltage which by inserting or removing the capacitor from the circuit will affect the circulating current.

Alternatively, Bergna *et al.* [66] proposes a control methods based on the representation model used in [79]. The method consist in using a feed-forward technique to eliminate the voltage disturbance caused by the output current.

4.5 Circulating Current Suppression

Unbalanced voltages between the MMC arms introduces a high 2^{nd} harmonic component which increases the RMS value of the current, the SM voltage ripple and the converter losses. Thus this component impacts the rating of SM capacitors and semiconductor devices [79]. Circulating currents can be eliminating by introducing an active control using PI controllers such as the proposed in [76, 79, 80]. The 2^{nd} harmonic component is suppressed in theses cases indirectly by means of arm voltages. The study described in [66] eliminates this harmonic component by using a resonant proportional integral controller with the reference generated by filtering the sum of all capacitor voltages.

Along with control strategies the undesired circulating current can be reduced by means of design the inductor at a given current peak value [51] or by inserting a main-circuit filter (resonant filter) [56, 57, 81]. These methods are described in the Chapter 3 of this thesis.

5 Simulation Models

Due the high number of non-linear elements present in a MMC the simulation time required when using DMs, which uses extremely accurate models to represent IGBTs, increases rapidly as the number of submodules raise. Likewise, the amount of time taken into the process of creating or modify an simulation schematic is also an enormous drawback when only the overall response is necessary to analyze. The computational effort needed unleashed the use of reduced-order models capable of reproduce with enough accuracy the behavior reposes of switches, controls and the converter itself by using simpler elements or controlled sources [82, 83].

A wide range of AVMs has been developed for different applications and purposes. Whether preserve switching details or neglect them in order to use larger integration time steps, requiring less computational resources resulting in a shorter simulation time [84]. Its use focusing in HVDC systems and VSC topologies can be found in [67, 68, 69, 85].

As example of its use in MMCs simulations, Peralta *et al.* [19] examine the dynamic performance of DM and AVM in a 401-level DSC-MMC. The AVM used showed to be at least 370 times faster than the DM. Although, it has been concluded the DM is preferable to observe high frequencies transients. Other uses can be found in [24, 26, 70] where the model used in [24] promoted a speedup from 250% (simulating 2 submodules per arm) to 31107% (simulating 120 submodules per arm) into the run time using PSCAD software.

Depending on the application, topology, control complexity, transients to be analyzed and desired run time different AVM can be used. Six of them will be presented in descending complexity order.

5.1 Type I: Physics-Based Models [86, 87, 88, 89, 90, 91, 92]

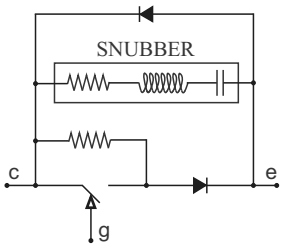
The development of these models are based on the mathematical model of an IGBT using differential equations. As example, Strollo [91] presented a model based on non quasi-static BJT model and a short-channel MOSFET model. As other example, Hefner [92] uses a model with variable resistors, variable and saturate capacitors, a BJT and a MOSFET to represent the dynamic behavior of the IGBT.

Despite the high accuracy of these models, they are complex requiring small time steps making its use in MMC simulations inappropriate.

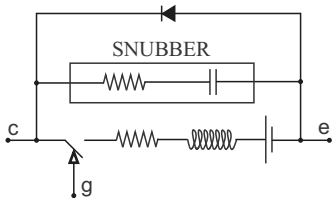
5.2 Type II: Detailed Nonlinear IGBT-Based Model [19]

This model is configured using a controlled switch, two diodes and a RCL snubber circuit as shown in Figure 10(a). In this model, the IGBT turns on when the collector-emitter voltage is greater than the diode forward voltage (Vf) and the gate signal is applied. It turns off when the gate signal is removed or when the collector-emitter voltage is lower than Vf. When the current drives in the opposite direction it passes trough the anti-parallel diode.

Variations in it can be found such as the model used by MatLab/Simulink, Figure 10(b). The IGBT is modeled using a controlled switch, an anti-parallel diode, a resistance (representing the ON-resistance), an inductor, a dc source (representing the IGBT saturation voltage) and a RC snubber circuit. The turn-on and turn-off requirements for this model are the same as described in the previous paragraph.



(a) Detailed model using a diode.



(b) Detailed model using a series resistor, inductor and dc-source.

Figure 10 – Detailed models.

As the model cover all characteristics of an IGBT including: reverse blocking capability, switching events (including in some models the fall time and tail time), conduction losses and block states, this model has been used as reference. As the number of SMs increase the number of switches and diodes to be simulated and small time steps are required to represent the switching pattern. This leads in a high computational effort and its use becomes undesirable. Nevertheless, simulations with a small number of SMs can still use this model. This model is then used especially in simulations that require high accuracy such as the ones used to test circuit protections, where any change on the physical variables (e.g. voltage, current and heat dissipation) needs to be predicated.

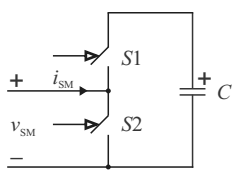
5.3 Type III: Simplified IGBT-Based Model

Also known as ideal switch model its molded in the principle that the IGBT works as a ideal switch with a small on-resistance R_{ON} (in the range of $m\Omega$) and a large off-resistance R_{OFF}[93]. Although the majority of this models it represents the switching IGBT behavior, the non-linearity caused by the anti-parallel diode is not taken into account. A more realistic model can be found where the switch is replaced by a variable resistor and his value depends on the gate signal, collector-emitter voltage and current direction.

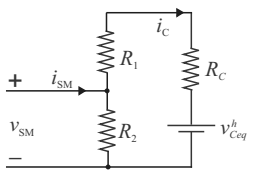
A HBSM using this model is presented in Figure 11(a) where $S1$ and $S2$ are the IGBT models. Because of its configuration the simulation model is used for most applications but the ones listed for the Type II.

5.4 Type IV: Thévenin Equivalent Circuit [24, 70]

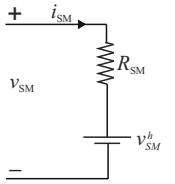
The SM model is provided by creating a Thévenin equivalent circuit for each MMC SM. The SM capacitor in then replaced by a voltage source in series with a resistance [94]. This substitution results in a model that



(a) HBSM using a simplified IGBT-based model.



(b) HBSM using a discretized capacitor.



(c) HBSM using a thévenin equivalent circuit.

Figure 11 – HBSM models.

requires a small number of operations and accept a longer time step.

Using the trapezoidal discretization method the capacitor submodule C is replaced by a voltage history source v^h_{Ceq} in series with a resistance $R_C = \Delta t/2C$, where Δt is the time step used in the simulation. Based on the trapezoidal integration method

$$v_C(t) = \frac{1}{C}\int_0^t i_C(t) \approx v_C(t-\Delta t) + \frac{\Delta t}{2}\frac{i_C(t-\Delta t) + i_C(t)}{C} \tag{5.1}$$

therefore

$$v_C(t) = R_C \cdot i_C(t) + v^h_{Ceq}(t-\Delta t) \tag{5.2}$$

where

$$v^h_{Ceq}(t-\Delta t) = R_C \cdot i_C(t-\Delta t) + v_C(t-\Delta t). \tag{5.3}$$

Substituting the capacitor in the Type III model results in the representation presented in Figure 11(b). The individual HBSM Thévenin equivalent circuit can be derivative by using

$$v_{SM}(t) = R_{SM}(t) i_{SM}(t) + v^h_{SM}(t-\Delta t) \tag{5.4}$$

where

$$R_{SM}(t) = \frac{R_2(t)(R_1(t)+R_C)}{R_1(t)+R_2(t)+R_C} \tag{5.5}$$

$$v^h_{SM}(t-\Delta t) = v^h_{Ceq}(t-\Delta t)\frac{R_2(t)}{R_1(t)+R_2(t)+R_C} \tag{5.6}$$

and R_1 and R_2 the variable resistances from the Type III IGBT model, resulting on the circuit presented on Figure 11(c).

Since the N SMs in a MMC arm are connected in series and the current i_{SM} is the same in all the SMs this model provides a way to represent this connection as a Thevinin equivalent where its resistance and voltage are given by

$$R_{arm}(t) = \sum_{i=1}^{N} R_{SM_i}(t) \tag{5.7}$$

$$v_{arm}(t) = \sum_{i=1}^{N} v_{SM_i}(t) = \left(\sum_{i=1}^{N} R_{SM}(t)\right) i_{SM}(t) + \sum_{i=1}^{N} v^h_{SM}(t-\Delta t). \tag{5.8}$$

The introduction of this modeling approach allows a simple representation of a MMC with a high number of SMs. Yet, it is necessary record all individual capacitor voltages and each switch state in order to determine the submodule resistance and equivalent voltage. Although the simplification used here this model is used mostly only in software where the solution technique is based on the Thevenin method.

5.5 Type Va: AVMs Based on Switching Functions [19, 95]

Using AVMs, the IGBT is not equivalent represented but the SM behavior is presented using controlled voltage and current sources and diodes. The use of AVMs generally lays on the principle that all SM capacitor voltages are balanced, MMC variables are controlled and harmonics (especially second order) in the circulating current are suppressed. Thus, while using those models the balancing control and circulating current control can be neglected.

Complex AVMs can be used to represent harmonic content of switching events and cover the converter losses. Also the use of AVMs is not restrict to any modulation technique.

As some examples of high accuracy AVMs lets consider the model used by PLECS [95] shown in Figure 12. In the model the dc-side (where the capacitors or voltage sources are connected) is the right side of the model while the ac-side (where the SMs are connected in series) is represented by the left part. The inputs are the IGBT gate signals, 0 or 1 representing ON and OFF states respectively. The respective circuit configuration is shown in Figure 13

Using the HBSM AVM, Figure 12, the voltage across the ac-side are dependent of the ac-side current direction, dc-side voltage and IGBTs gate signals. The voltage is either $v1$ or $v2$ defined as

$$v1 = (g2 - 1)Vdc \tag{5.9}$$

$$v2 = (g1)Vdc, \tag{5.10}$$

where $g1$ and $g2$ are the IGBT gate signals in Figure 13(a) and Vdc the voltage at the dc-side terminals. The current at the dc-side is for instance $i1$ or $i2$, where

$$i1 = (g2 - 1)I + \tag{5.11}$$

$$i2 = (g1)I-, \tag{5.12}$$

with $I+$ and $I-$ representing the ac-side current. In this model, $I+$ is different from zero when the current flows from the + terminal to the - terminal and $I-$ is different from zero when the current flows in the opposite direction.

Using the same idea, for the FBSM AVM, the ac-side voltage is either

$$v1 = (g2 + g3 - 1)Vdc \tag{5.13}$$

$$v2 = (g1 + g4 - 1)Vdc, \tag{5.14}$$

where $g1$, $g2$, $g3$ and $g4$ are the IGBTs gate signals in Figure 13(b). The dc-side current is them one of the following current sources depending on the current direction an the ac-side terminals:

$$i1 = (g2 + g3 - 1)I + \tag{5.15}$$

$$i2 = (g1 + g4 - 1)I - . \tag{5.16}$$

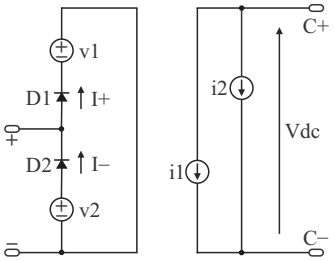


Figure 12 – High accuracy AVM for HBSM and FBSM.

(a) HBSM. (b) FBSM.

Figure 13 – Equivalent SM configuration.

It can be demonstrate these model correct represent the SMs behavior using all combinations of IGBT gate signals and ac-side current directions. These models correctly accounts blanking times (i.e. when both IGBTs in one SM leg are turned off), discontinuous conduction mode (e.g. when charging the capacitor via the reverse diodes) [95]. As consequence these models can support all the controllers described before but because its average behavior variables such as the arm current can not be correctly represented.

5.6 Type VIa: Generic AVMs Based on Switching Functions

A simpler representation can be used in order to model a SM by considering the IGBTs as a bidirectional switch. Besides, in order to represent HBSM and FBSM it is necessary to consider the IGBTs in the same leg are complementary. In these circumstances the SM can be represented as shown in Figure 14 where

$$\begin{cases} v = (g)Vdc, \\ i = (g)I, \end{cases} \tag{5.17}$$

and g is a 'equivalent' gate signal.

In order to represent the HBSM the gate signal is

$$\begin{cases} g = 1 & \text{if } g1 = 1 \; and \; g2 = 0, \\ g = 0 & \text{if } g1 = 0 \; and \; g2 = 1. \end{cases} \tag{5.18}$$

Using FBSM for instance

$$\begin{cases} g = 1 & \text{if } g1 = g4 = 1 \text{ and } g2 = g3 = 0, \\ g = -1 & \text{if } g1 = g4 = 0 \text{ and } sg2 = g3 = 1 \\ g = 0 & \text{otherwise.} \end{cases} \tag{5.19}$$

As these models represents the IGBT as simple switches its use should be considered with precaution and used mainly in the initial design tests.

5.7 Type Vb and VIb: AVMs Based on Fundamental Frequency [95]

These models use the same circuits as shown in Type Va and VIa models. The main difference is use of IGBTs duty cycles as control signals instead IGBTs gate signals. Thus the modulators, e. g. triangular carrier based PWM, are not required in the simulation. Because the duty cycle generally is accurately generating using large time steps this model can use time steps as large as the inverse of the switching frequency.

As the duty cycle is used, the series connection of N SMs can replaced by a single model with a capacitor $C_{eq} = C/N$ and a voltage $v_{eq} = Nv_C$. Thus, this configuration is preferable in simulation with high switching frequency or high number of SMs. Although it does not present the switching behavior of the SMs, suppressing harmonics in both dc and ac-side. Also the balancing control in this case should be taken into account carefully since the switching behavior was totally removed.

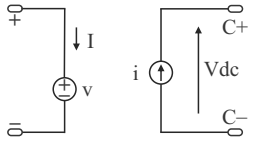


Figure 14 – Equivalent AVM representation for HBSM ans FBSM.

6 Performance Study

This chapter will compare the different simulation models in a HB-MMC. The index proposed will evaluate the accuracy of each model compared to a real prototype implemented. Finally the simulation time required will be presented.

6.1 Simulation Index

Along with the fast development of technology used to build new electronic devices such as the MMC or new components e.g., the use of simulation software to predicate different variables in an application, i.e. current, voltage or a control variable have been increasingly adopted. Morgan and Jones [96] presents the main software used in different fields e.g. As another example, Wipke *et al.* [97] demonstrate a simulation of a vehicle performance using ADVISOR. With the intention to simulate a wide range of applications different models of nonlinear elements were developed, such as for a diode [98], an insulated-gate field-effect transistor (IGFET) [99] and a battery [100, 101]. Using these models complex devices like a Photovoltaic (PV) array [102, 103] or a wind turbine [104].

Due the fast implementation of simulation software an index to represent the accuracy of a simulation has not been presented yet , neither for element models, a hardware control representation (i.e. a PI controller or a synchronizing circuit [105] e.g.) nor a complete set-up (a buck converter e.g. [106]). The indexes proposed in this thesis can be used to measure the deviation (positive and negative) between simulation results or between the simulation and experimental results which can be used to compare result from different models.

6.1.1 Index Calculation

As example to show how generate the indexes consider the two signals in Figure 15 where there is a generic reference signal (solid line) and the signal simulated (dotted line).

As can been seen there are moments where the reference signal is greater in amplitude than the simulated signal as there are moments where the reference signal have a lower amplitude. The 'index signal' is then

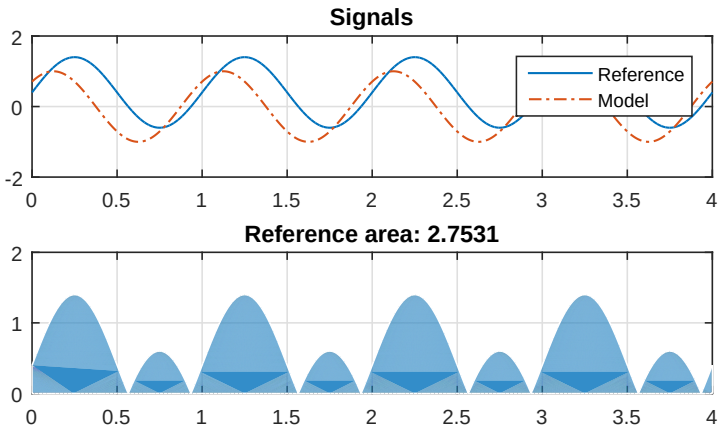


Figure 15 – Example signal (phase: $\pi/4$).

divided into two parts, the positive difference where the model is greater and the negative difference where the opposite occurs. Then the signals are used to calculate the positive and negative indexes, i_p and i_n. By combining the signals the total and the mean indexes, i_{total} and i_{mean} can be calculated. To do so the signal's areas are calculated as show in Figure 16, with the reference area described in Figure 15. Finally the four index values are calculated using

$$i_p = \frac{positive\ area}{reference\ area} \tag{6.1}$$

$$i_n = \frac{negative\ area}{reference\ area} \tag{6.2}$$

$$i_{total} = \frac{positive\ area + negative\ area}{reference\ area} \tag{6.3}$$

$$i_{mean} = \frac{positive\ area - negative\ area}{reference\ area}. \tag{6.4}$$

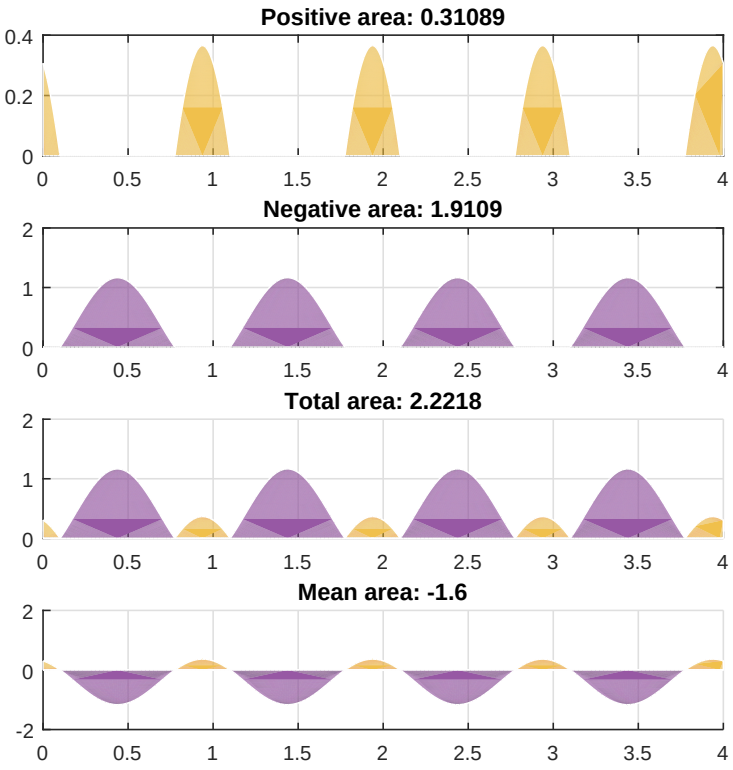


Figure 16 – Difference areas of the signal in Figure 15.

From the example given above it is obtain:

$$i_p = \frac{0.31089}{2.7531} = 11.2924\%$$
$$i_n = \frac{1.9109}{2.7531} = 69.409\%$$
$$i_{total} = \frac{0.31089 + 1.9109}{2.7531} = \frac{2.2218}{2.7531} = 80.7018\%$$
$$i_{mean} = \frac{0.31089 - 1.9109}{2.7531} = \frac{-1.6}{2.7531} = -58.1163\%,$$

which indicates the deviation from the reference.

6.1.2 Comparison

The most used analysis nowadays is the Fast Fourier transform (FFT) which represent a signal in the frequency domain. The FFT for the signal in Figure 15 is presented in Figure 17.

Now if the model signal in Figure 15 was phase shifted by $-\pi/4$ it would give the same indexes as the signal analyzed before indicating the signals are similar, which is true. However it can not be easily verified using the FFT tool. The FFT of those signal have the same amplitude spectrum but a completely different phase spectrum. The phase spectrum makes it difficult to analyze. This may lead us to conclude that one of the models are wrong, but since we are discussing the model accuracy the models are equally correct (or wrong).

Thus, it can be said the FFT is the best tool to present the frequencies in a signal while a time-based index seems more useful to compare signals. Other advantage is the simplicity of the index calculation since there is no need to use the frequency domain only a matter of area calculation. Other advantage of its use is when a signal with with a high number of frequencies is analyzed, which results in a FFT with a high number of components or when the signals samples are not equal time-spaced making the FFT use impossible.

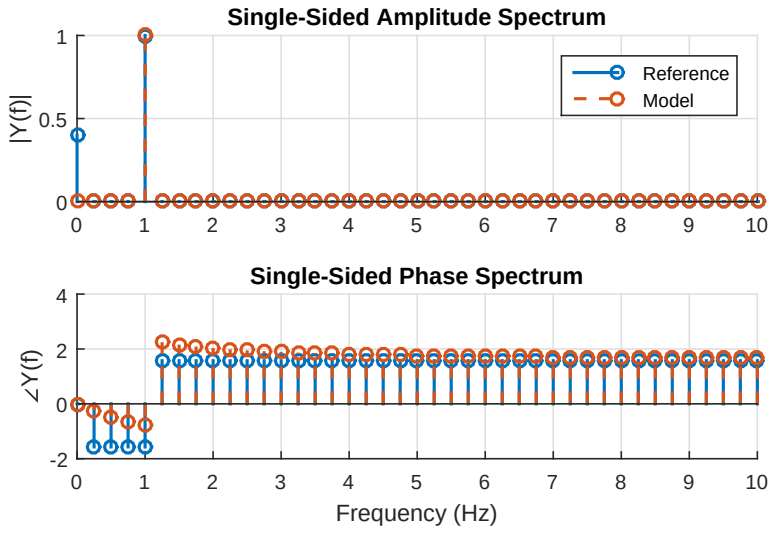


Figure 17 – FFT of the signals in Figure 15.

6.2 Results

The evaluating topology used is presented in Figure 18. It consists in a HB-MMC using HB-SM connected to a RL load. The model used has 4 SMs per arm with a capacitance $C = 6\text{mF}$, arm inductance $l = 1.8\text{mH}$ (the inductor resistance is equal to 300mH). The dc-bus voltage E is 240V, and the PWM frequency is 312Hz. The prototype uses a MOSFET with Fet resistance equals to 100mΩ and the anti-parallel diode has a on-resistance of 10mΩ. The control used is a direct modulation which is a open-loop modulator based on PWM approach [107]. The controller was discretized in $2 \cdot N \cdot fc$ while the current and voltage measurements where taken using a quantization of 10 bits. With this strategy only the reference voltage is sent to the submodule which in this case is equal to $E/8(1 + sin(100\pi t)$. The PWM approach uses phase-shifted triangular waves with correspondent phase-shift as given by Li *et al.* [108] with the objective to reduce harmonics in the output voltage, for this case was used a displacement angle of 90 ° between SMs adjacent in a arm and a displacement angle of 45 ° between same SMs in different arms.

The first test was realized considering a constant load consisting in a resistor R of 14.2Ω and a inductor L of 1.54mH. The results obtain using different simulation models are presented in Figure 19. The Type V and Type VI are divided into two sub-models which consist in the models of Figure 12 (Type Va and VIa) and Figure 14 (Type Vb and VIb). The index results for each signal compared with the detailed model (Type II) can be found in Table 10 in Appendix B.

The second test was made by changing the resistor on the load from 36.5Ω to 18.3Ω, at the dashed line, which elevates the arm currents and consequently the capacitor voltage ripples. Besides the transient can be observable into those results as shown in Figure 20. A zoom has been applied to the arm current in order to expose the transient. The indexes for this simulation are shown in Table 11 in Appendix B.

The simulations are made on a computer with AMD Phenom(tm) II N970 Quad-Core Processor 2.20 GHz, 6,00Gb of RAM memory and a Windows 7 operational system of 64 bits using Simulink on MatLab R2015a. The average required time for each simulation (using normal mode) to represent each second of MMC operation using time steps of $6.26ms$ is shown in Table 1.

From the results and the indexes presented in the two Tables the reader can verify which model is suitable for its own application. E.g. the Types V and VI does not represent with enough precision the arm currents and because that its use is not recommended for simulate protection techniques or heat dissipation.

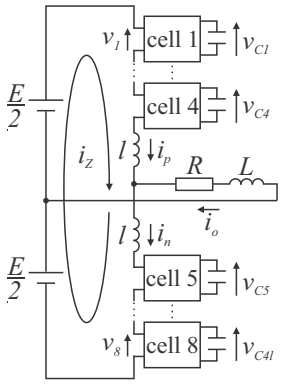
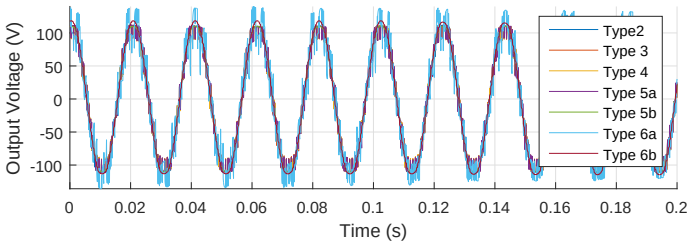


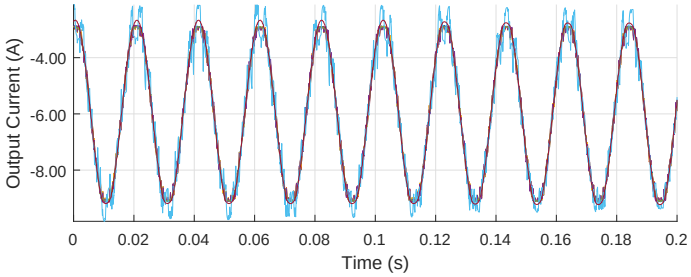
Figure 18 – HB-MMC with 4 submodules per arm.

Table 1 – Required time for simulation of the HB-MMC

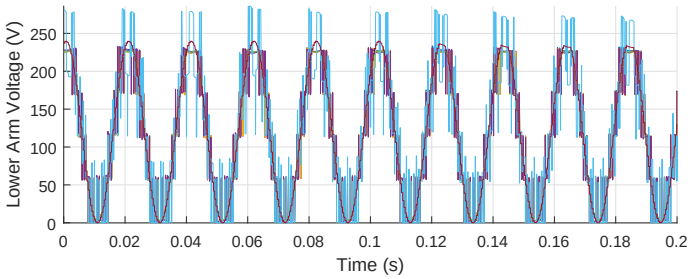
Simulation Model	**Time (s)**	**Percentage (%)**
Type II	48.9729	100
Type III	16.1965	33.0724
Type IV	19.4549	39.7259
Type Va	46.5098	94.9706
Type Vb	20.8628	42.6007
Type VIa	29.5278	60.2942
Type VIb	10.5573	21.5574



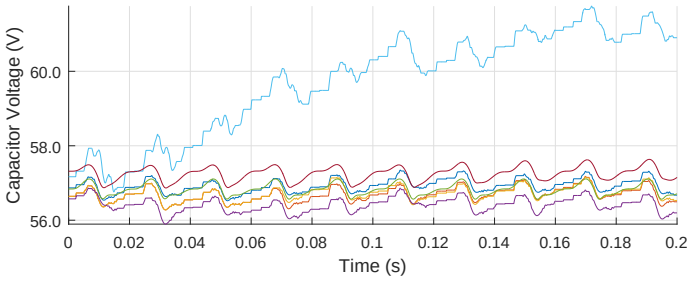
(a) Output Voltage.



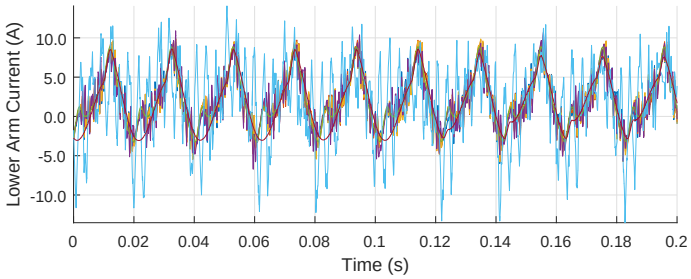
(b) Output Current.



(c) Lower Arm Voltage.

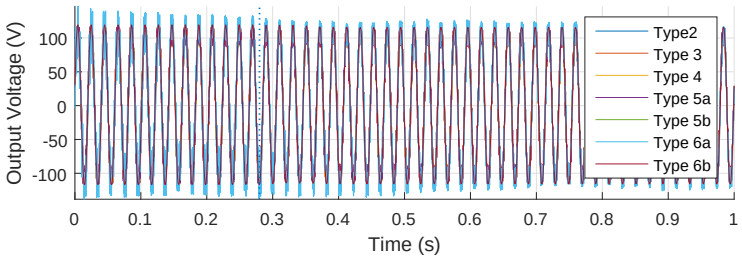


(d) Capacitor Voltage.

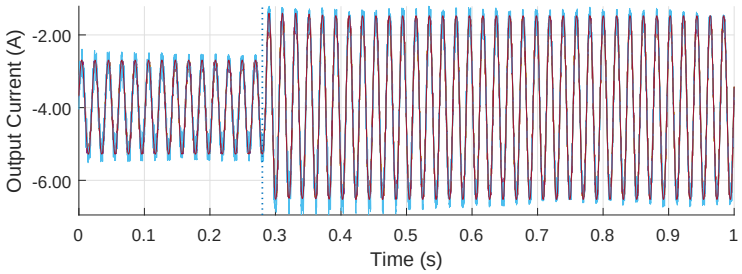


(e) Lower Arm Current.

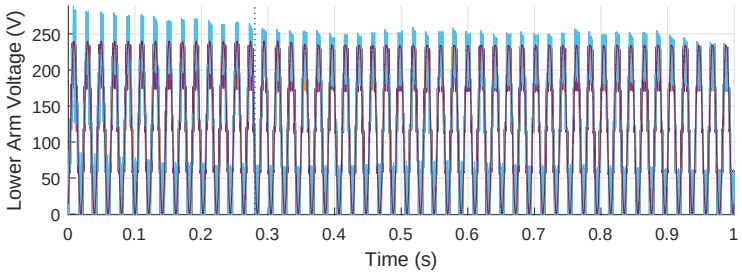
Figure 19 – Simulation results with constant load.



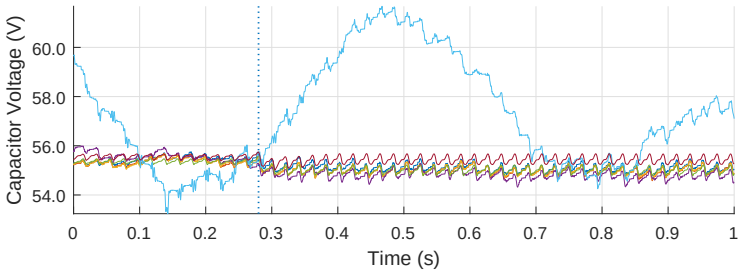
(a) Output Voltage.



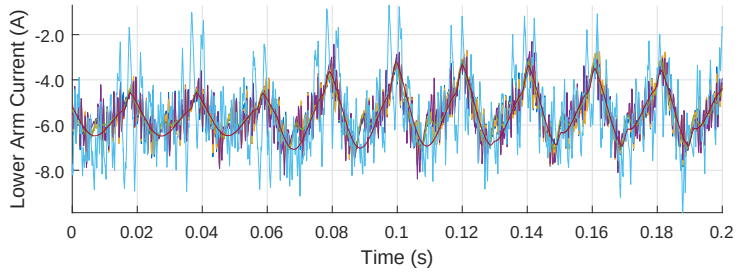
(b) Output Current.



(c) Lower Arm Voltage.



(d) Capacitor Voltage.



(e) Lower Arm Current.

Figure 20 – Simulation results with variable load.

7 State-Space Representation

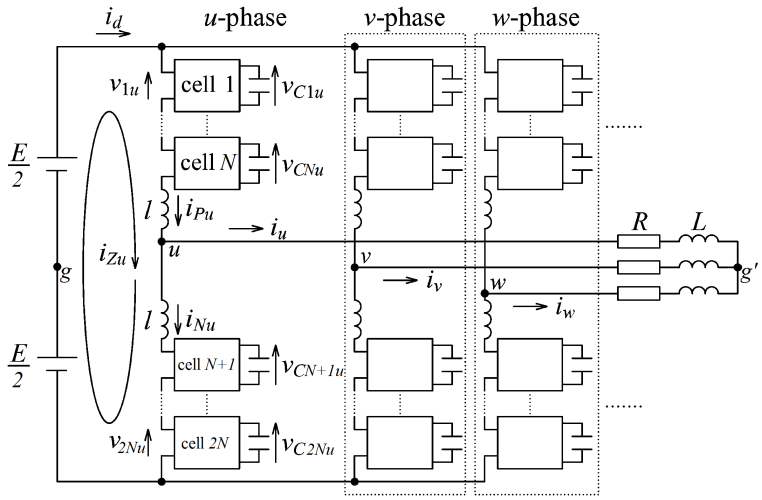
7.1 MMC Topology

The study of state-space representation in this section is focused on the DSC-MMC. Figure 21(a) shows the schematic for this topology. The most used submodule topologies are the half-bridge and single-phase full-bridge, whose schematics are shown in Figure 21(b) and 21(c).

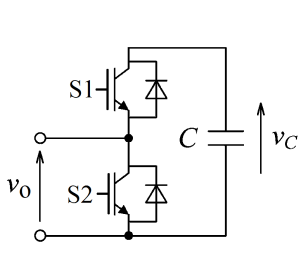
Figure 21(a) shows a converter with N submodules connected in cascade per arm ($2N$ submodules per leg). Thus, depending on the topology and the IGBTs switching state the correspondent capacitor is connected to the circuit [27].

The output submodules voltage levels (v_o) and all switching states considered for both half-bridge (Figure 21(b)) and full-bridge (Figure 21(c)) topologies are listed in Table 2.

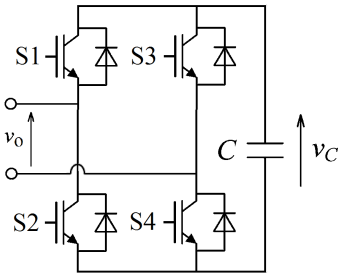
As shown in Figure 21(a) the MMC has an arm inductor l in order to protect the components when the converter is turned on (the capacitors are discharged), to protect the components in fault conditions and to decrease arm current oscillations [10, 28]. A resistance r, to simulate losses in the arm, can be connected in series with the arm inductance. Finally, a load (RL) is connected between the arms in each leg.



(a) Multi-phase circuit.



(b) Half-bridge cell.



(c) Full-bridge cell.

Figure 21 – Circuit schematic of a double-star type multilevel converter.

Table 2 – Switching submodule states.

Topology	Switching states				v_o
	S1	S2	S3	S4	
Half-bridge	ON	OFF	X	X	v_C
	OFF	ON	X	X	0
Full-bridge	ON	OFF	OFF	ON	v_C
	OFF	ON	ON	OFF	-v_C
	ON	OFF	ON	OFF	0
	OFF	ON	OFF	ON	0

The goal of this chapter is to simulate a single-phase and three-phase MMC with half-bridge submodules using state-space representation and comparing the results with a DM model. The same method can be applied to a multi-phase MMC and/or different submodules topologies with minimal changes. The g point (load) is necessary to be connected with the midpoint bus g' for a single-phase MMC and optional for a multi-phase [29].

7.2 MMC Control Method

The control used on this work aims to maintain the submodules capacitor with constant voltage, to control the circulating current (i_Z) and to switch each submodule to create a desired load voltage. The complete voltage control description for each one of the submodules capacitors is proposed in [28] and can be divided in: averaging control and balancing control.

7.2.1 Averaging control

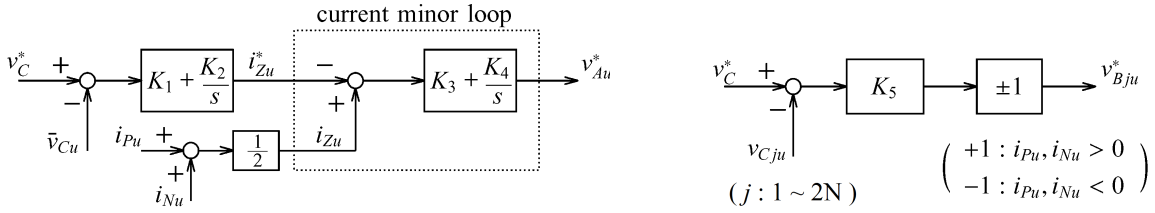
A block diagram for the averaging control for u-phase is shown in Figure 22(a). The outer loop is responsible for controlling the averaging voltage $\overline{v}_{Cu}$ given by

$$\overline{v}_{Cu} = \frac{1}{2N}\sum_{j=1}^{2N} v_{Cju}, \tag{7.1}$$

where the index j represent the submodule number, with respective capacitor voltage v_{Cju} and v_C^* the capacitor voltage set point.

The outer loop gives the reference for the circulating current, i_{Zu}^*responsible to charge the capacitors connected to the circuit by the submodules. Since i_{Zu} is a circulating current, impossible to measure, it can be calculated by

$$i_{Zu} = \frac{1}{2}\left(i_{Pu} + i_{Nu}\right), \tag{7.2}$$



(a) Averaging control. (b) Balancing control.

Figure 22 – Block diagrams of a MMC control [28].

where i_{Pu} and i_{Nu} are the upper and lower arm current respectively. The inner loop, on the other hand forces the $i_{Zu}$to follow the reference i^*_{Zu}. When this happen it is possible to control $\overline{\mathrm{v}}_{\mathrm{Cu}}$ without affecting the load current i_u given as follows:

$$i_u = \ i_{Pu} - \ i_{Nu}. \tag{7.3}$$

Continuous mathematical equations for either outer or inner loop are described as:

$$i^*_{Zu} = K_1 \left(v^*_C - \overline{v}_{Cu}\right) + K_2 \int_0^t \left(v^*_C - \overline{v}_{Cu}\right) dt, \tag{7.4}$$

$$v^*_{Au} = K_3 \left(i_{Zu} - i^*_{Zu}\right) + K_5 \int_0^t \left(i_{Zu} - i^*_{Zu}\right) dt \tag{7.5}$$

in a time instant t. The MMC and the control are turned on in $t = 0$.Thus, when $v^*_C > \overline{v}_{Cu}$, the reference i^*_{Zu}increases, and the inner loop results in a command v^*_{Au} with the objective to charge the capacitors.

7.2.2 Balancing control

Figure 22(b) shows a u-phase balancing control for each submodule indicated by the index j. The balancing control is used to select what submodules will be inserted to the circuit. Capacitors with the lowest voltage will be inserted in the circuit when the upper and lower currents (i_{Pu} and i_{Nu}) are positive, for the upper arm and lower arm respectively, charging the capacitors.

Hence, submodules with higher capacitors voltage will be inserted when i_{Pu} and i_{Nu} are negative, discharging the capacitors. The use of balancing control is recommended for better voltage control based on the principle described above.

The continuous mathematical expression for balancing control, when $j = 1 \ : N$ is described as

$$v^*_{Bju} = sign\left(i_{Pu}\right) K_5 \left(v^*_C - v_{Cju}\right) \tag{7.6}$$

while for $j = N + 1 \ : 2N$, $v^*{}_{Bju}$ is described as

$$v^*_{Bju} = sign\left(i_{Nu}\right) K_5 \left(v^*_C - v_{Cju}\right) \tag{7.7}$$

where $sign(\cdot)$ is the signum function.

Finally, the individual reference voltage v^*_{ju}, for PWM modulation is expressed as:

$$v^*_{ju} = v^*_{Au} + \ v^*_{Bju} - \frac{v^*_u}{N} + \frac{E}{2N} \ \ (j = 1 : N) \tag{7.8}$$

$$v^*_{ju} = v^*_{Au} + v^*_{Bju} + \frac{v^*_u}{N} + \frac{E}{2N} \ \ (j = N + 1 : 2N) \tag{7.9}$$

where v^*_u is the reference for the load ac-voltage and E the voltage supply.

At this point the voltage command v^*_{ju} is normalized by its respective capacitor voltage v_{Cju}, followed by PWM modulation. The carrier wave used in the PWM is a triangular waveform having maximum value of unity and minimal value of zero and frequency f_C. Each submodule has its own carrier wave but they are lagging of $360\hat{\mathrm{A}}^{\mathrm{o}}/2N$ to each other. This is strongly recommended to reduce the total harmonic influences on the load voltage and to produce a phase-voltage with a total of $(2N{+}1)$-level voltage with a frequency of $2Nf_C$ [28].

7.3 Mathematical Model

7.3.1 State-space equations

Recreating the MMC circuit with state-space equations we will first consider a single-phase MMC constituted by 2 submodules per arm and a resistance r in series with the inductor l. The IGBTs for this model will be substituted by switches since it is not the objective of this thesis verify the effects of them in the circuit.

Firstly, the circuit within all the submodules inserted (Figure 23(a)) is considered. From this circuit, the capacitors voltage variations are described as:

$$\frac{dv_{C1u}}{dt} = \frac{dv_{C2u}}{dt} = \frac{i_{Pu}}{C} \tag{7.10}$$

$$\frac{dv_{C3u}}{dt} = \frac{dv_{C4u}}{dt} = \frac{i_{Nu}}{C} \tag{7.11}$$

where C is the submodule capacitor. From Kirchhoff's voltage law we obtain:

$$\frac{E}{2} - \ v_{C1u} - v_{C2u} - ri_{Pu} - l\frac{di_{Pu}}{dt} - Ri_u - L\frac{di_u}{dt} = 0 \tag{7.12}$$

$$\frac{E}{2} + Ri_u + L\frac{di_u}{dt} - ri_{Nu} - l\frac{di_{Nu}}{dt} - v_{C3u} - v_{C4u} = 0. \tag{7.13}$$

Substituting i_u from (7.3) in (7.12) and (7.13), we have

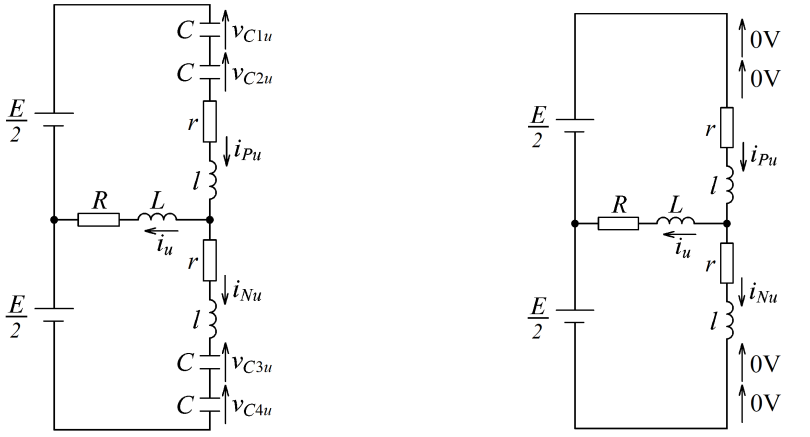
$$L\frac{di_{Nu}}{dt} = (L+l)\frac{di_{Pu}}{dt} + v_{C1u} + v_{C2u} + (R+r)\,i_{Pu} - Ri_{Nu} - E/2 \tag{7.14}$$

$$L\frac{di_{Pu}}{dt} = (L+l)\frac{di_{Nu}}{dt} + v_{C3u} + v_{C4u} - Ri_{Pu} + (R+r)\,i_{Nu} - E/2. \tag{7.15}$$

Solving the system given by (7.14) and (7.15) for $\frac{di_{Pu}}{dt}$ and $\frac{di_{Nu}}{dt}$, results in

$$\frac{di_{Pu}}{dt} = \frac{-(L+l)(v_{C1u}+v_{C2u}) - L(v_{C3u}+v_{C4u}) - [r(L+l)+Rl]\,i_{Pu} + (Rl-rL)\,i_{Nu} + (2L+l)\,E/2}{2Ll+l^2} \tag{7.16}$$

$$\frac{di_{Nu}}{dt} = \frac{-L(v_{C1u}+v_{C2u}) - (L+l)(v_{C3u}+v_{C4u}) + (Rl-rL)\,i_{Pu} - [r(L+l)+Rl]\,i_{Nu} + (2L+l)\,E/2}{2Ll+l^2} \tag{7.17}$$



(a) All submodules inserted.

(b) All submodules bypassed.

Figure 23 – Equivalent circuits for different submodules inserted.

Using (7.10), (7.11), (7.16) and (7.17) the state-space continuous representation can be described in terms of

$$\dot{X} = AX + BU \tag{7.18}$$

where

$$U = [E] \tag{7.19}$$

$$X = \begin{bmatrix} v_{C1u} & v_{C2u} & v_{C3u} & v_{C4u} & i_{Pu} & i_{Nu} \end{bmatrix}^T \tag{7.20}$$

$$B = \begin{bmatrix} 0 & 0 & 0 & 0 & E/2l & E/2l \end{bmatrix}^T \tag{7.21}$$

$$A = \frac{1}{2Ll + l^2} \begin{bmatrix} 0 & 0 & 0 & 0 & \left(2Ll + l^2\right)/C & 0 \\ 0 & 0 & 0 & 0 & \left(2Ll + l^2\right)/C & 0 \\ 0 & 0 & 0 & 0 & 0 & \left(2Ll + l^2\right)/C \\ 0 & 0 & 0 & 0 & 0 & \left(2Ll + l^2\right)/C \\ -(L+l) & -(L+l) & -L & -L & -\left[r\left(L+l\right) + Rl\right] & Rl - rL \\ -L & -L & -(L+l) & -(L+l) & Rl - rL & -\left[r\left(L+l\right) + Rl\right] \end{bmatrix}. \tag{7.22}$$

With all capacitors out of the circuit (Figure 23(b)), the right part of (7.10) and (7.11) are equal to zero since there is no current flowing through the capacitors. Using the same method as before for (7.12) and (7.13) we will obtain the same equations but without the capacitors voltages. Thus, in this case (7.16) and (7.17) do not have the capacitors voltages leading to rewrite A in (7.22) as

$$A = \frac{1}{2Ll + l^2} \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\left[r\left(L+l\right) + Rl\right] & Rl - rL \\ 0 & 0 & 0 & 0 & Rl - rL & -\left[r\left(L+l\right) + Rl\right] \end{bmatrix}. \tag{7.23}$$

In this case the circuit and the capacitors are represented by (7.18), (7.19), (7.20), (7.21) and (7.23).

At this point it is developed by a simple association a state-space continuous representation for a MMC with a total of N submodules per arm. Comparing (7.22) and (7.23) it is possible to see the term that multiples the current through the capacitors in the capacitor voltages variations (lines 1 to 4) are $1/C$ when connected to the circuit and zero when disconnected. Also, the terms that multiply the capacitors voltages in the current variations (lines 5 and 6) are either $-(L+l)/(2Ll+l^2)$ or $-L/(2Ll+l^2)$ when the capacitor is connected to the circuit and zero when disconnected.

Hence, using

$$z_j = \begin{cases} 1, & C_j \textit{ is connected} \\ 0, & C_j \textit{ is disconnected} \end{cases}, \tag{7.24}$$

the state-space continuous representation for both 3 and none capacitors connected can be expended to N

submodules per arm and any number of capacitors connected by (7.18), (7.19), and:

$$X = \begin{bmatrix} v_{C1u} & v_{C2u} & \cdots & v_{C2Nu} & i_{Pu} & i_{Nu} \end{bmatrix}^T \tag{7.25}$$

$$B = \begin{bmatrix} 0 & 0 & \cdots & 0 & E/2l & E/2l \end{bmatrix}^T \tag{7.26}$$

$$A = \frac{1}{2Ll + l^2} \begin{bmatrix} 0 & \cdots & 0 & 0 & \cdots & 0 & z_1\left(2Ll + l^2\right)/C & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & 0 & \cdots & 0 & z_N\left(2Ll + l^2\right)/C & 0 \\ 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & z_{N+1}\left(2Ll + l^2\right)/C \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & z_{2N}\left(2Ll + l^2\right)/C \\ -z_1(L+l) & \cdots & -z_N(L+l) & -z_{N+1}L & \cdots & -z_{2N}L & -\left[r\left(L+l\right) + Rl\right] & Rl - rL \\ -z_1 L & \cdots & -z_N L & -z_{N+1}(L+l) & \cdots & -z_{2N}(L+l) & Rl - rL & -\left[r\left(L+l\right) + Rl\right] \end{bmatrix} \tag{7.27}$$

For the purpose of using this equation in mathematical software it is required a state-space discrete representation, such as

$$x\left[k+1\right] = ax\left[k\right] + bu[k] \tag{7.28}$$

for each iteration k. $x[k]$ and $u[k]$ are the values of X and U in the iteration k and:

$$a = \Delta T A + I \tag{7.29}$$

$$b = \Delta T B \tag{7.30}$$

where ΔT is the timestep used between each iteration and I an identity matrix with the same dimension as A.

Since the matrix A depends on the capacitors connected to the circuit z and it can change based on the control result, the matrix a can also change at each iteration and need to be recalculated

Each phase of a three-phase MMC with the g point interconnected with the g' point can be represented with the same state-space representation as described above.

7.3.2 MMC control

To control the MMC in a discrete state, (7.1)-(7.9) are also discretized. The discretization of an integral $w(t)$, such as the ones used in (7.4) and (7.5) can be defined as

$$r\left(t\right) = \int_0^t w(t)dt \cong r\left[k+1\right] = r\left[k\right] + \Delta T w\left[k\right] \tag{7.31}$$

when the instant t is equal to a integer multiple of ΔT and $r\left[1\right]$ (first iteration) is zero. The normalized reference voltage $v_{ju}^*[k]$ is used now to connect or disconnect the capacitor by

$$z_j[k] = \begin{cases} 1, & v_{ju}^*[k] \geq cw_j[k] \\ 0, & v_{ju}^*[k] < cw_j[k] \end{cases} \tag{7.32}$$

where cw_j is the PWM carrier wave for each submodule.

7.4 Results

The AVM proposed on this thesis was simulated with different MMC configurations to be compared with the DM. Both models are simulated using an incremental time of 100μs and a sinusoidal wave with rms value

of V_o as the reference load voltage v_u^*, using the software MATLab/Simulink. The performance analysis on three different MMC simulated is shown in the next sections.

7.4.1 Single-phase MMC with 4 submodules

Table 3 and Table 4 show the circuit parameters and control gains used for the simulation of a single-phase MMC with a total of 4 submodules ($2N$) under steady state conditions [28].

Figure24 shows the simulated waveforms for both DM and AVM. As can be seen in Figure24 the waveforms from the state-space representation reproduce correctly the MMC behavior comparing to the DM model. There is a difference between the models in the capacitor voltage (Figure24(f)) but it is at the range of 2V or 2.9% of the capacitor voltage set point (70V).

The other waveforms however present just a small difference between the models. Those divergences can be explained by the switching losses due the IGBTs presents in the DM model or even the solver method used.

7.4.2 Single-phase MMC with 8 submodules

Table 5 and Table 6 show the circuit parameters and control gains used for the simulation of a single-phase MMC with a total of 8 submodules ($2N$) under steady state conditions [28].

The load rms voltage V_o for this simulation was changed from 3.18 kV to 1.27 kV at 495 ms in aim to study the AVM transient behavior.

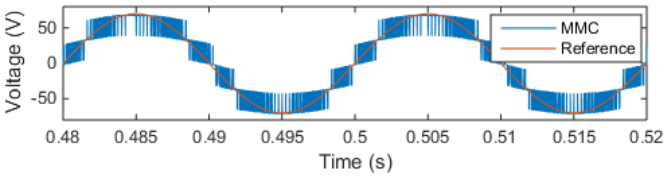
Figure25 shows the simulated waveforms for the AVM and DM as showed for the single-phase MMC with 4 submodules. The AVM simulated reproduces correctly the MMC behavior under both normal and transient operation. The most visible difference is at the capacitor voltage (Figure25(d)), but at the range of 10 V which represents only 0.44% of the capacitor voltage set point (V_C). The load current (Figure25(c)) waveforms are overlapped.

Table 3 – Circuit Parameters Used for Simulation.

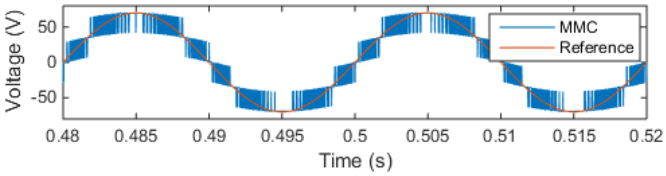
DC supply voltage	E	140 V
Rated rms voltage	V_o	50 V
Rated frequency	$_f$	50 Hz
Submodule capacitance	C	3 mF
Capacitor voltage	Vc	70 V
Arm resistance	r	100 mΩ
Arm inductance	l	1 mH
Load resistance	R	10 Ω
Load inductance	L	2 mH
Power factor	$\cos\phi$	0.9 at 50Hz
Carrier frequency	f_C	8 kHz
Equivalent switching frequency	$4f_C$	32 kHz

Table 4 – Control Gains Used for Simulation.

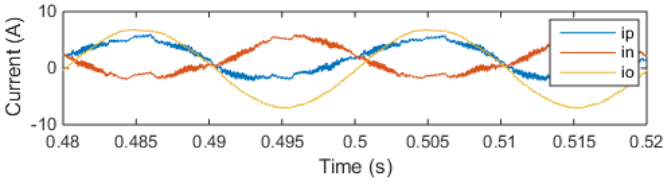
Proportional gain of averaging control	K_1	0.5 A/V
Integral gain of averaging control	K_2	80 A/(V·s)
Proportional gain of current control	K_3	1 A/V
Integral gain of current control	K_4	640 A/(V·s)
Proportional gain of balancing control	K_5	0.5



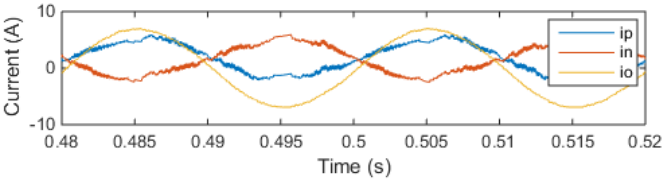
(a) Load voltage and reference from the AVM.



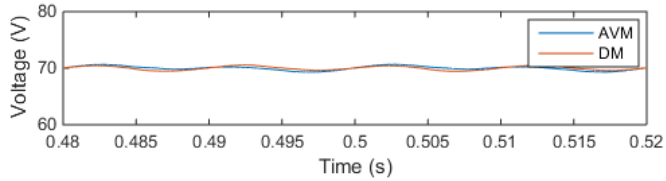
(b) Load voltage and reference from the DM.



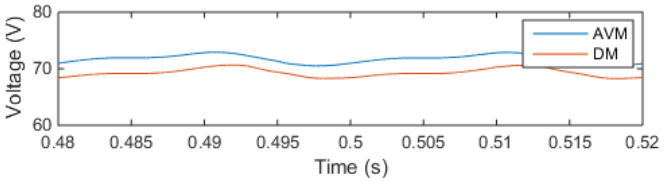
(c) Upper and lower arms and load current from the AVM.



(d) Upper and lower arms and load current from the DM.



(e) Average capacitor voltage.



(f) Upper capacitor voltage.

Figure 24 – Simulated waveforms for a single-phase MMC with 4 submodules.

Table 5 – Circuit Parameters Used for Simulation.

DC supply voltage	E	9 kV
Rated frequency	$_f$	50 Hz
Submodule capacitance	C	1.9 mF
Capacitor voltage	Vc	2.25 kV
Arm resistance	r	100 mΩ
Arm inductance	l	3 mH
Load resistance	R	30 Ω
Load inductance	L	6 mH
Power factor	$\cos\,\phi$	0.9 at 50Hz
Carrier frequency	f_C	2 kHz
Equivalent switching frequency	$8f_C$	16 kHz

Table 6 – Control Gains Used for Simulation.

Proportional gain of averaging control	K_1	0.5 A/V
Integral gain of averaging control	K_2	150 A/(V·s)
Proportional gain of current control	K_3	1.5 A/V
Integral gain of current control	K_4	150 A/(V·s)
Proportional gain of balancing control	K_5	0.35

7.4.3 Three-phase MMC with 8 submodules per arm

Figure26 shows the simulated waveforms for the AVM and DM of a three-phase MMC with 8 submodules per leg and the g and g' point (Figure 21) interconnected. The phase to ground circuit parameters used for this simulation is described in Table 5. Table 6 shows the control gains used. The phase to ground load rms voltage V_o was 3.18 kV. At 500 ms a load with resistance of 30 Ω and inductance of 6 mH was connected in parallel to the previous load.

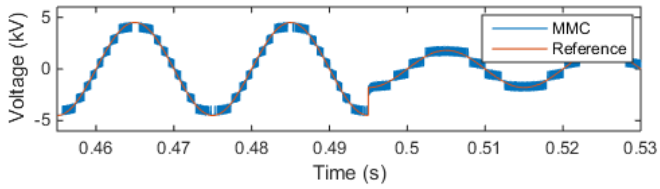
Figure 26(c) and 26(d) show the active and reactive power required by the three-phase load. The red and yellow curves represent the power required by the MMC load connected to a three-phase voltage source with phase to ground rms voltage of V_o. The DM model is showed again to be accurate to represent the MMC even at the transient states as can be seen on Figure 26(c) and 26(d). The deviation on the capacitor voltage now is at maximum value of 4V representing 0.17% of the capacitor voltage set point.

7.4.4 Processing time

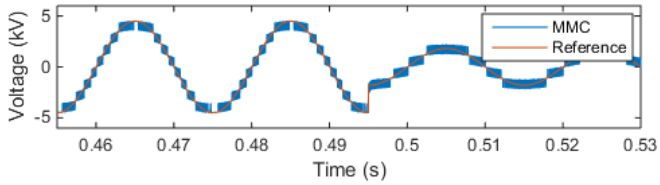
Computing time for each simulated models described in the sections above were measured for a 1 s simulation time. The simulations were performed on a computer with 2.3 GHz Intel Core i5-2410M processor, 6 GB of RAM and 64 bits system. Table 7 shows the averaging processing time required for each model. The results show that the AVM developed requires between 32.8% and 71.4% the processing time required to simulate the DM.

Table 7 – Processing time required.

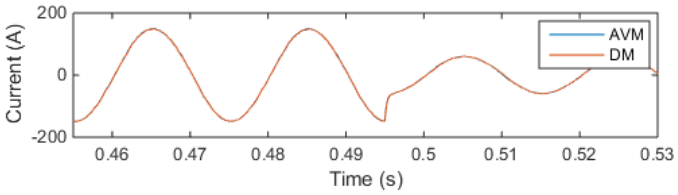
MMC	**AVM**	**DM**
Single-phase with 4 submodules	15.39 s	33.19 s
Single-phase with 8 submodules	16.28 s	49.61 s
Three-phase with 8 submodules	95.35 s	133.61 s



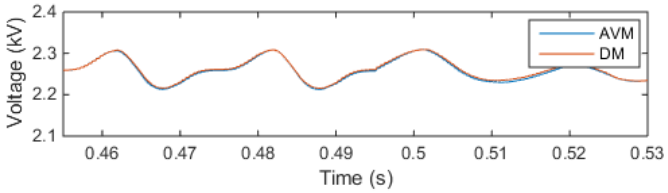
(a) Load voltage and reference from the AVM.



(b) Load voltage and reference from the DM.

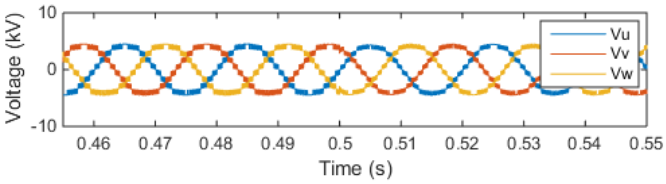


(c) Load current

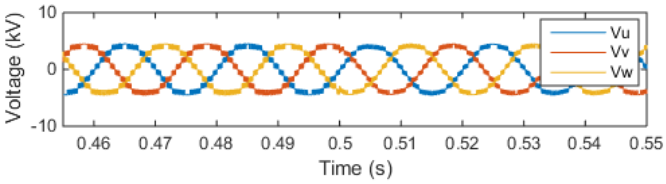


(d) Upper capacitor voltage.

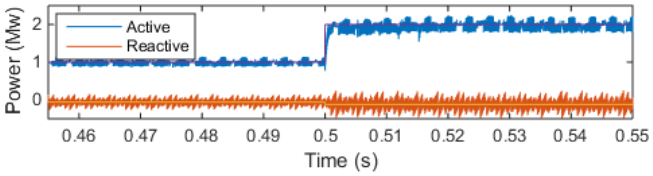
Figure 25 – Simulated waveforms for a single-phase MMC with 8 submodules.



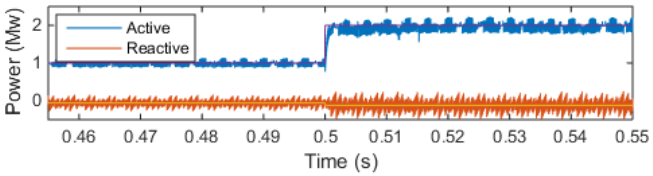
(a) Load voltage and reference from the AVM.



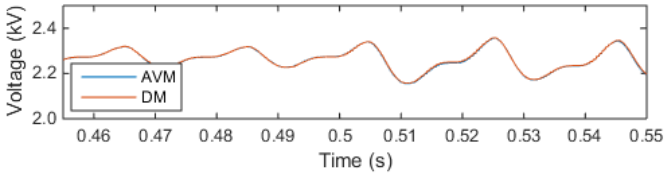
(b) Load voltage and reference from the DM.



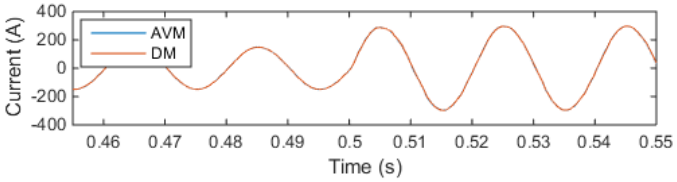
(c) Active and reactive load power from the AVM.



(d) Active and reactive load power from the DM.



(e) Upper capacitor voltage.



(f) Current load for one phase.

Figure 26 – Simulated waveforms for a three-phase MMC with 8 submodules per arm

8 Conclusion

The MMC has being the subject of several studies which provided great improvements into HVDC applications. These improvements are leading the MMC to achieved any voltage requirements for a widely range of applications. Thus, new MMC and SM topologies, control and even simulation techniques are being developed to maximize the efficiency of the MMC in each application.

In order to provide an MMC overview this thesis has shown some of the most used MMC designs, including SM topologies. Components sizing were covered along with respective goals: such as the limitation of the energy and voltage ripples in the SM capacitor, and arm inductor sizing to suppress current ripples, current rise and high frequency components of arm currents. MMC and SM protection circuits, with the objective to secure the MMC components under fault conditions, are also carried out. Nevertheless, the use of filters to improve the MMC output quality was approached.

The most used control techniques were covered including current and voltage control and the balancing control used in this converter topology to keep the capacitors in each submodule with the same voltage. The different simulation modules are presented and discussed its use for different proposes. An index was proposed in order to evaluate the accuracy of each simulation model and a performance study was presented.

Even though some of the most used MMC design and sizing have being covered here, specific applications may require different topologies or sizing methods from those discussed in this thesis. The reader is then encouraged to seek different and new MMC studies to fulfill their requirements.

From the second part of this work, it was demonstrated the principles to create a state-space representation of single and three-phase MMC with $2N$ submodules per leg. Advantages and disadvantages of use an AVM besides a DM were presented and discussed. The results and the processing time required for each model were compared for accuracy.

The presented model is useful to researches and engineers who are using simulation tools to study the MMC control.

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APPENDIX A – MMC and SM Topologies Comparation

Table 8 – Comparison of Various MMC Topologies.

	DSC-MMC	**Dual-MMC**	**SSC-MMC**	**SDC-MMC**
Circulating current	Yes	Yes	No	Yes
Voltage in unbalance condition	-	-	Higher than SDC	-
Current in unbalance condition	-	-	-	Higher than SSC
Voltage in balance condition	2/phase	2/phase	1/phase	$\sqrt{3}$/phase
Current in balance condition	$\sqrt{3}$/phase	$\sqrt{3}$/phase	$\sqrt{3}$/phase	1/phase
Capacitor size under balanced conditions	-	Higher than DSC	Higher than SDC	Lower than SSC
Capacitor size under unbalanced conditions	-	-	Lower than SDC	Higher than SSC
Hardware complexity	-	Higher than DSC	Lowest	-
Controller complexity	Easier than SSC	Medium-Hard	Medium	Easier than SSC

Table 9 – Comparison of Various SM Topologies [39].

SM circuit	**HBSM**	**FBSM**	**3LSM-FC**	**3LSM-NPC**	**CDSM**	**5LCCSM**
Voltage levels	$0, v_c$	$0, \pm v_c$	$0, v_{c1}, v_{c2}, (v_{c1} - v_{c2})$	$0, v_{c2}, (v_{c1} + v_{c2})$	$0, v_{c1}, v_{c2}, (v_{c1} + v_{c2})$	$0, v_{c1}, v_{c2}, \pm(v_{c1} + v_{c2})$
DC-fault-handling capability	No	Yes	No	No	Yes	Yes
No. of capacitors per arm	20	20	20	20	20	20
No. of SMs per arm	20	20	10	10	10	10
No. of IGBTs per arm(inserting/bypassing)	40	80	40	40	40	40
No. of extra IGBTs per arm (conducting)	0	0	0	0	20 ($S5$)	40 ($S5$ and $S6$)
No. of extra diodes per arm	0	0	0	40	40	0
Estimated power losses	0.69%	0.96%	0.83%	0.83%	0.83%	0.83%
Extra power losses compared to the HBSM	0	39%	20%	20%	20%	20%

APPENDIX B – Index Results

Table 10 – Index results from the signals on Figure 19.

Signals	**Type III**		**Type IV**		**Type Va**		**Type Vb**		**Type VIa**		**Type VIb**	
	i_p	i_n	i_p	i_n	i_p	i_n	i_p	i_n	i_p	i_n	i_p	i_n
Output Voltage	0.0062	0.0062	**0.0061**	**0.0059**	0.0160	0.0162	0.0402	0.0407	0.1034	0.1093	0.0452	0.0421
Output Current	0.0055	0.0055	**0.0054**	**0.0052**	0.0122	0.0125	0.0210	0.0215	0.0821	0.0878	0.0278	0,0247
Arm Voltage	**0.0043**	**0.0043**	0.0047	0.0046	0.0129	0.0130	0.0650	0.0655	0.1115	0.1144	0.0698	0.0675
Capacitor Voltage	0	0.0103	0	0.0092	0	0.0223	0.0003	0.0047	0.1209	0	0.0142	0.0005
Arm Current	**0.0635**	**0.0659**	0.0638	0.0663	0.1014	0.1102	0.1590	0.1569	0.5211	0.5923	0.1646	0.2329

Table 11 – Index results from the signals on Figure 20

Signals	**Type III**		**Type IV**		**Type Va**		**Type Vb**		**Type VIa**		**Type VIb**	
	i_p	i_n	i_p	i_n	i_p	i_n	i_p	i_n	i_p	i_n	i_p	i_n
Output Voltage	0.0036	0.0036	**0.0035**	**0.0034**	0.0147	0.0148	0.0418	0.0418	0.0879	0.0857	0.0442	0.0431
Output Current	0.0034	0.0034	**0.0033**	**0.0033**	0.0111	0.0113	0.0254	0.0254	0.0684	0.0667	0.0287	0,0278
Arm Voltage	**0.0029**	0.0029	**0.0029**	0.0029	0.0123	0.0124	0.0659	0.0658	0.0742	0.0726	0.0678	0.0670
Capacitor Voltage	0	0.0046	0	0.0044	0.0019	0.0096	**0.0004**	0.0046	0.0939	0.0064	0.0112	**0.0001**
Arm Current	0.0726	0.0724	**0.0713**	**0.0709**	0.1567	0.1621	0.2291	0.2310	0.5772	0.6346	0.2422	0.2998